

Thermal Annealing Effects on Copper Microstructure in Through-Silicon-Vias

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ABSTRACT

In this paper, we have studied the microstructure evolution of one-year room-temperature-aged Through-Silicon Via (TSV) copper after annealing the TSV samples at 300 °C, 400 °C and 500 °C for 180 minutes. Hardness and elastic modulus values are obtained by using nano-indentation technique. The hardness and elastic modulus values decrease as annealing temperature increases. The microstructure of copper (Cu) is examined to obtain grain size and texture, using electron backscatter diffraction (EBSD). Copper grain growth, if any, is studied under different annealing temperatures. There was no observable grain growth for the annealing temperatures studied in this work. Moreover, microstructure variation at different locations within a Cu TSV is also studied.

KEY WORDS: EBSD, electroplated copper, microstructure evolution, nano-indentation, thermal annealing, TSV

INTRODUCTION

Copper through-silicon via (TSV) is an enabling technology for 3D integration, playing an important role in connecting stacked dice. Increasingly, TSVs with a diameter ranging from 100 μm, 50 μm, 10 μm, or less are being pursued by industry. The microstructure of electroplated copper will be dependent on the TSV diameter, as the diameter shrinks in size. Annealing the TSVs at high temperatures typically changes the grain size and orientation, resulting in additional changes in material properties such as hardness. Annealing the Cu TSV reduces the residual stress as well as Cu pumping and associated reliability issues in subsequent thermal excursions.

The performance of transistors is sensitive to stresses induced by the integration of Cu TSV in a chip. In metal-oxide-semiconductor field-effect transistor (MOSFET) devices, a stress of 100 MPa can change the carrier mobility by over 7% [28]. There are a few studies done on the microstructure and mechanical behavior of Cu TSV after annealing [1, 26, 27], while there are a lot of studies available on the mechanical behavior and reliability aspects of Cu TSVs [2-5, 12-24]. There is only limited study on the long-term aging of Cu TSVs. In this paper, the effect of long-term aging followed by high-temperature annealing on the microstructure and mechanical properties of aged Cu TSV is experimentally studied.

SAMPLE PREPARATION

Cu TSV samples were fabricated using a conventional cleanroom process. The silicon wafer was 500 μm thick and had uniformly distributed 50-μm diameter blind TSVs with 250 μm depth. Copper was electroplated from a seed layer deposited on the side wall of a blind TSV. Upon electroplating, the silicon substrates were diced into a number of samples for molding and microstructure analysis. The over-plated Cu was not polished off. The Cu TSV samples were stored in room temperature (e.g. 25 °C) and cross-sectioned to be characterized after one year. The cross-sectioned TSV samples were polished using colloidal silica solution and mechanical planarization to obtain a smooth planar surface. The electron backscatter diffraction (EBSD) was performed to characterize grain size and texture, while nano-indentation was performed to characterize the hardness and elastic modulus.

EXPERIMENTAL PROCEDURE

Annealing effects were studied by EBSD and Nano-indentation analysis. Since Cu recrystallization occurs at 250 °C [6, 7], annealing temperature was chosen above 250 °C. This ensures that the temperature is high enough to let microstructure recrystallization. Three annealing temperatures were 300 °C, 400 °C and 500 °C with 180 minutes of annealing for each temperature.

Nano-indentations were carried out using a Nano-indenter (MTS XP System® equipped with the continuous stiffness measurement attachment). During the indentation process, the applied load and the displacement were continuously recorded. A three-sided pyramidal diamond Berkovich tip to a maximum depth of 1000 nm. There are six indentations, starting from 5 μm from the top edge with a spacing of 20 μm along the axis of the TSVs (Figure 1). The spacing was selected so as to minimize the influence from other neighboring indents as well as the influence of surrounding silicon walls. The elastic modulus and hardness values were obtained from the test by using the Oliver-Pharr relation [8].

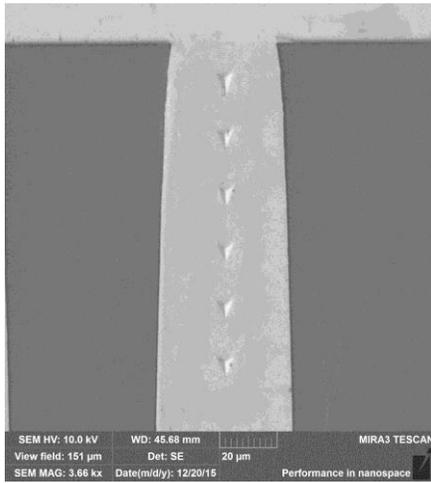


Fig. 1 SEM image showing the indentation spots along the axis of a polished blind TSV

EBSD measurements were carried out using a TESCAN SEM® equipped with an EBSD detector. The samples were angled 70° towards the electron-scanning microscopy (SEM) detector while taking the EBSD measurements. All EBSD images were rectangular in shape with 120 μm length along the axis of the TSV and 60 μm width along the transverse width or radial direction of the TSV. EBSD measurements were first taken on the cross-sectioned samples, and then the samples were subjected to high-temperature annealing treatments. It is important to study the cross-sectioned samples under vacuum condition or flowing argon gas to prevent copper oxidization. Therefore, the annealing treatments were accomplished using Cambridge Fiji Plasma® atomic layer deposition (ALD) tool that is capable of providing such operating conditions. The cross-sectioned Cu TSVs were placed in the chamber with a ramp of 13 °C/minute under vacuum and flowing argon gas at 20 sccm throughout the annealing process. After letting the Cu TSVs cool down under vacuum environment, the second post-annealing EBSD measurement was conducted on the same TSV. By comparing the two EBSD images, before and after annealing, the crystal structure changes due to annealing could be determined.

RESULTS AND DISCUSSION

The hardness values of the Cu TSVs under one-year room-temperature-aged condition as well as after three high-temperature annealing conditions were measured and compared. Fifteen Cu TSVs with six indentations per TSV were studied for each annealing condition. Thus, 90 indentation measurements were averaged and compared. The one-year room-temperature-aged samples had the highest hardness value of 1.4 GPa. This hardness value is higher than the reported values of bulk copper ($H \sim 1.0\text{-}1.2$ GPa). This can be explained by factors such as induced residual stress during electroplating, inclusion of additives during electroplating process [10, 11, 25], and smaller copper grain size in TSV trench compared to bulk copper [29, 30]. Figure 2 compares the average hardness values for as-received, one-year room-temperature-aged samples as well as three high-temperature-

annealed samples. After annealing, the hardness value decreases to 1.2 GPa, 1.1 GPa and 1.0 GPa as the annealing temperature increases. This reduction in hardness can be explained through reduced residual stress. Hall-Petch relation cannot be applied [9], since the grain size did not increase, as shown in Figures 4, 5 and 6. Since the samples were room-temperature aged for one year, it is possible that Cu microstructure had already fully stabilized, and no further grain growth occurred due to high-temperature annealing. The only thing that was observed was that some of the grains had minor changes in their orientation after high-temperature annealing. Here, the explanation for reduction in measured hardness values lies in the presence of residual stresses after electroplating, and these residual stresses decrease due to high-temperature annealing. Thus, the hardness values seem to be more influenced by the residual stresses rather than by the grain size.

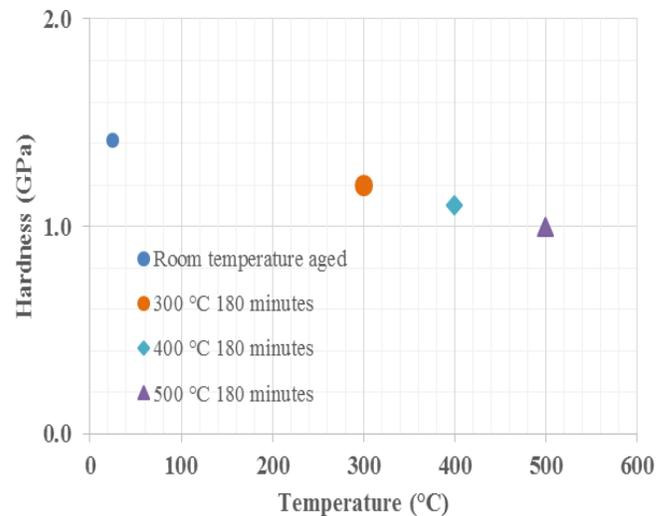


Fig. 2 Average Hardness Values Before and After High-Temperature Annealing

Figure 3 compares the average E-modulus values for as-received one-year-aged samples as well as three high-temperature-annealed samples. As in hardness values, the modulus before high-temperature aging was 111 GPa, and the modulus reduced to 102 GPa, 96 GPa and 94 GPa after high-temperature thermal aging. As mentioned earlier, the grain size did not change, and there was minor change in the grain orientation. This grain orientation change is driven by the decrease in total free energy since microstructures tend to reach to lowest total free energy for maintaining stable states [1].

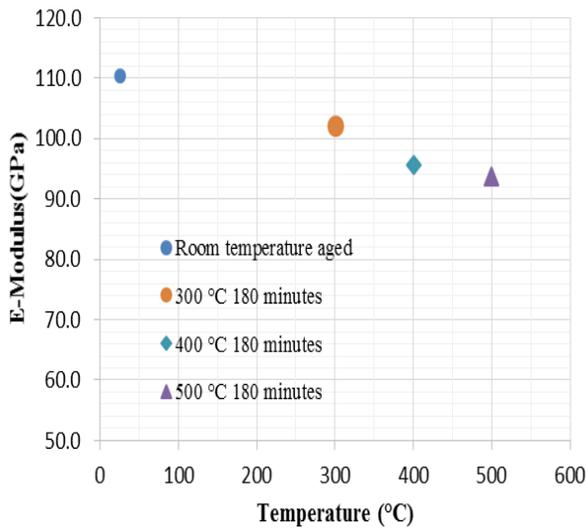


Fig. 3 Average E-modulus Values Before and After High-Temperature Annealing

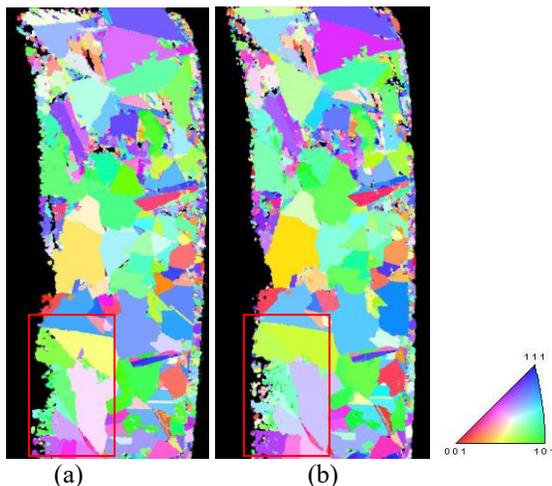


Fig. 4 EBSD Images: (a) Aged at Room Temperature for One Year, and (b) Annealed at 300 °C for 180 minutes.

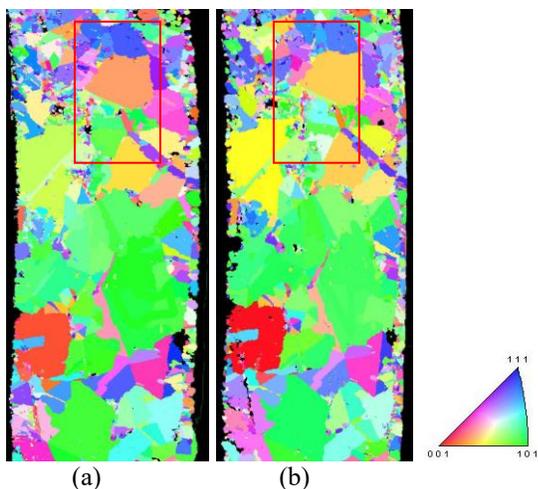


Fig. 5 EBSD Images: (a) Aged at Room Temperature for One Year, and (b) Annealed at 400 °C for 180 minutes.

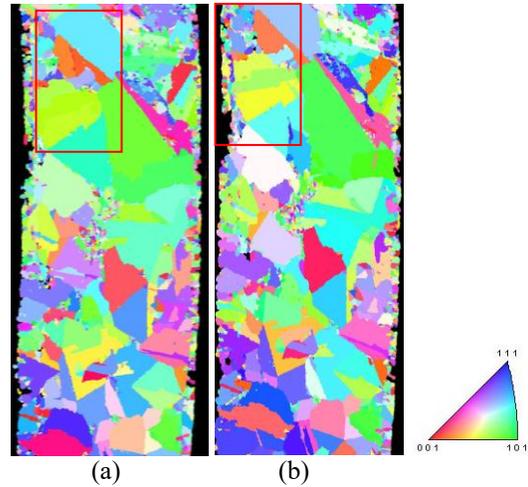


Fig. 6 EBSD Images: (a) Aged at Room Temperature for One Year, and (b) Annealed at 500 °C for 180 minutes.

To assure annealing duration is not the limiting factor for grain growth, the Cu TSVs were annealed at 400 °C for 30 hours. Figure 7 compares the sample before and after annealing. There is no significant grain growth observed. Also limited changes in grain orientation were observed. Based on this, it can be said that the annealing duration is not the limiting factor for grain growth. This confirms after one-year room-temperature aging, grain growth will not happen.

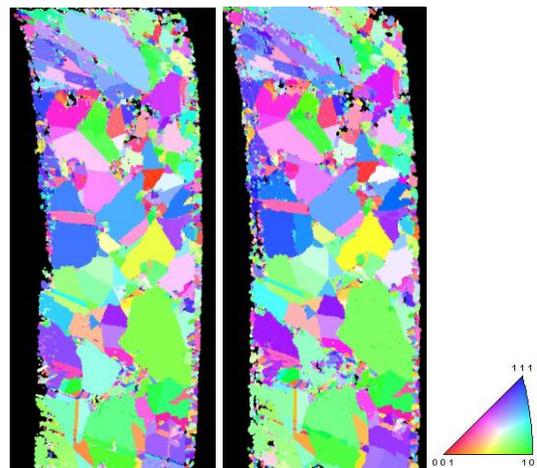


Fig. 7 EBSD Images: (a) Aged at Room Temperature for One Year, and (b) Annealed at 400 °C for 30 hours.

Additionally, the one-year-aged samples show a significant difference in grain size near the silicon walls and near the center of the TSVs, away from the silicon walls (Figure 8). The grains near the center of TSVs were about 10 – 20 μm in size, while the grains near the silicon walls were much smaller, about 2 μm in size.

The Cu seed-layer was deposited on the sidewall through physical-vapor-deposition (PVD). So the small grain on the side walls are the results of PVD process combined with electroplated copper within the holes of needle-shaped PVD region. Figure 9 shows an SEM image of the needle-shaped Cu seed layer, as deposited, prior to electroplating.

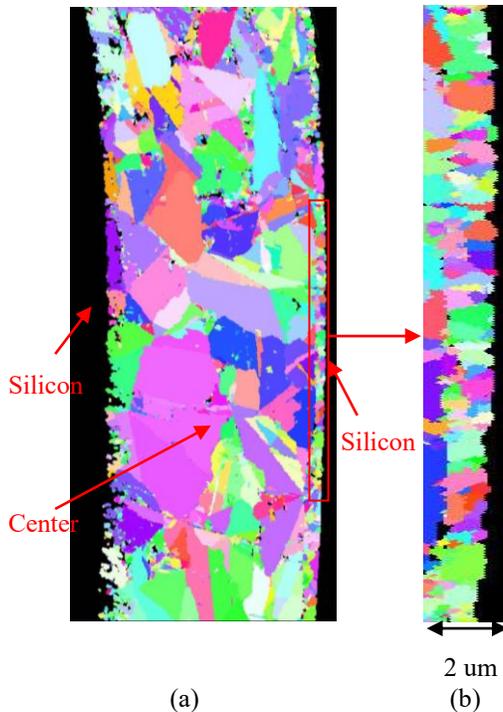


Fig. 8 EBSD Images: (a) Aged at Room Temperature for One Year, and (b) Detail of Edge

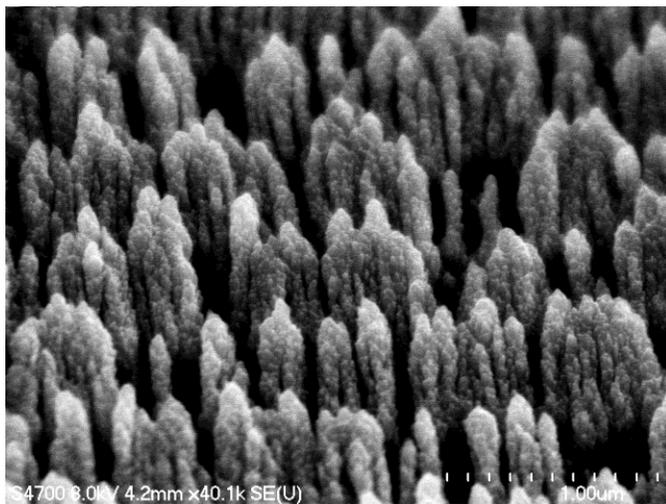


Fig. 9 SEM Image for Copper Seed Layer by PVD process

SUMMARY AND CONCLUSIONS

Cu TSVs that were aged at room temperature were used as starting samples in this study. The samples were then annealed at three temperatures 300, 400, and 500 °C over 180

minutes. The copper grain size distribution and texture were investigated using EBSD. The mechanical properties of Cu were investigated using nano-indentation to get hardness and elastic modulus values.

1. After one-year room-temperature aging, no further significant grain growth was observed after high-temperature annealing treatments.
2. After annealing treatments, the hardness and the elastic modulus decreased by 28% and 15% respectively. This reduction could be explained by possible relaxation of residual stresses enabled through the rotation of copper grains.

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REFERENCES

- [1] C. Okoro, K. Vanstreels, R. Labie, O. Luhn, B. Vandeveld, B. Verlinden, *et al.*, "Influence of annealing conditions on the mechanical and microstructural behavior of electroplated Cu-TSV," *Journal of Micromechanics and Microengineering*, vol. 20, p. 045032 (6 pp.), 04/ 2010.
- [2] P. Dixit, X. Luhua, M. Jianmin, J. H. L. Pang, and R. Preisser, "Mechanical and microstructural characterization of high aspect ratio through-wafer electroplated copper interconnects," *Journal of Micromechanics and Microengineering*, vol. 17, pp. 1749-57, 2007.
- [3] G. Changdong, X. Hui, and Z. Tong-Yi, "Fabrication of high aspect ratio through-wafer copper interconnects by reverse pulse electroplating," *Journal of Micromechanics and Microengineering*, vol. 19, p. 065011 (5 pp.), 06/ 2009.
- [4] X. Luhua, D. Pradeep, M. Jianmin, J. H. L. Pang, Z. Xi, K. N. Tu, *et al.*, "Through-wafer electroplated copper interconnect with ultrafine grains and high density of nanotwins," *Applied Physics Letters*, vol. 90, pp. 33111-1, 01/15 2007.
- [5] X. Luhua, P. Dixit, J. H. L. Pang, M. Jianmin, Z. Xi, T. King-Ning, *et al.*, "Characterization of nano-grained high aspect ratio through-wafer copper interconnect column," in *2007 Electronic Components and Technology Conference, 29 May-1 June 2007*, Piscataway, NJ, USA, 2007, pp. 2011-16.
- [6] T. Fischer, "Material science", New York, NY, 2009.
- [7] W. Weisbach, "Material Science", Wiesbaden, 2010
- [8] W. C. Oliver and G. M. Pharr, "An improved technique for determining hardness and elastic modulus using load and displacement sensing indentation experiments," *Journal of materials research*, vol. 7, pp. 1564-1583, 1992.
- [9] D. R. Askeland, "The Science and Engineering of Materials Self-Annealing", chapter 4, Pacific Grove, CA, 1984.[1]

- [10] X. Luhua, D. Pradeep, M. Jianmin, J. H. L. Pang, Z. Xi, [2-7]K. N. Tu, *et al.*, "Through-wafer electroplated copper interconnect with ultrafine grains and high density of nanotwins," *Applied Physics Letters*, vol. 90, pp. 33111-1, 01/15 2007.
- [11] S. Lagrange, S. H. Brongersma, M. Judelewicz, A. Saerens, I. Vervoort, E. Richard, *et al.*, "Self-annealing characterization of electroplated copper films," in *Third European Workshop on Materials for Advanced Metallization, 7-10 March 1999*, Netherlands, 2000, pp. 449-57.
- [12] X. Liu, P. A. Thadesar, C. L. Taylor, M. Kunz, N. Tamura, M. S. Bakir, *et al.*, "Thermomechanical strain measurements by synchrotron x-ray diffraction and data interpretation for through-silicon vias," *Applied Physics Letters*, vol. 103, p. 022107 (5 pp.), 07/08 2013.
- [13] C. Qiao, L. Xi, V. Sundaram, S. K. Sitaraman, and R. R. Tummala, "Double-Side Process and Reliability of Through-Silicon Vias for Passive Interposer Applications," *IEEE Transactions on Device and Materials Reliability*, vol. 14, pp. 1041-8, 12/ 2014.
- [14] L. Xi, C. Qiao, V. Sundaram, M. Simmons-Matthews, K. P. Wachtler, R. R. Tummala, *et al.*, "Reliability Assessment of Through-Silicon Vias in Multi-Die Stack Packages," *IEEE Transactions on Device and Materials Reliability*, vol. 12, pp. 263-71, 06/ 2012.
- [15] L. Xi, C. Qiao, V. Sundaram, R. R. Tummala, and S. K. Sitaraman, "Failure analysis of through-silicon vias in free-standing wafer under thermal-shock test," *Microelectronics Reliability*, vol. 53, pp. 70-8, 01/ 2013.
- [16] L. Xi, P. A. Thadesar, C. L. Taylor, O. Hanju, M. Kunz, N. Tamura, *et al.*, "In-situ microscale through-silicon via strain measurements by synchrotron x-ray microdiffraction exploring the physics behind data interpretation," *Applied Physics Letters*, vol. 105, p. 112109 (5 pp.), 2014.
- [17] L. Xi, P. A. Thadesar, C. L. Taylor, M. Kunz, N. Tamura, M. S. Bakir, *et al.*, "Dimension and liner dependent thermomechanical strain characterization of through-silicon vias using synchrotron x-ray diffraction," *Journal of Applied Physics*, vol. 114, p. 064908 (7 pp.), 08/14 2013.
- [18] X. Liu, M. Li, D. Mullen, J. Cline, and S. K. Sitaraman, "Design and assembly of a double-sided 3D package with a controller and a DRAM stack," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, pp. 1205-1212.
- [19] X. Liu, P. A. Thadesar, C. L. Taylor, M. Kunz, N. Tamura, M. S. Bakir, *et al.*, "Experimental Stress Characterization and Numerical Simulation for Copper Pumping Analysis of Through-Silicon Vias," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. PP, pp. 1-7, 2016.
- [20] X. Liu, Q. Chen, P. Dixit, R. Chatterjee, R. R. Tummala, and S. K. Sitaraman, "Failure mechanisms and optimum design for electroplated copper through-silicon vias (TSV)," in *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, 2009, pp. 624-629.
- [21] M. Jung, X. Liu, S. K. Sitaraman, D. Z. Pan, and S. K. Lim, "Full-chip through-silicon-via interfacial crack analysis and optimization for 3D IC," in *Proceedings of the International Conference on Computer-Aided Design*, 2011, pp. 563-570.
- [22] X. Liu, Q. Chen, V. Sundaram, S. Muthukumar, R. R. Tummala, and S. K. Sitaraman, "Reliable design of electroplated copper through silicon vias," in *ASME 2010 International Mechanical Engineering Congress and Exposition*, 2010, pp. 497-506.
- [23] X. Liu, M. Simmons-Matthews, K. P. Wachtler, and S. K. Sitaraman, "Reliable design of TSV in free-standing wafers and 3d integrated packages," in *ASME 2011 International Mechanical Engineering Congress and Exposition*, 2011, pp. 903-910.
- [24] X. Liu, Q. Chen, V. Sundaram, M. Simmons-Matthews, K. P. Wachtler, R. R. Tummala, *et al.*, "Thermo-mechanical behavior of through silicon vias in a 3D integrated package with inter-chip microbumps," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 1190-1195.
- [25] J. Gong, P. Vukkadala, J. K. Sinha, and K. T. Turner, "Determining local residual stresses from high resolution wafer geometry measurements," *Journal of Vacuum Science & Technology B*, vol. 31, p. 051205, 2013.
- [26] P. Saettler, M. Boettcher, and K. J. Wolter, "Characterization of the annealing behavior for copper-filled TSVs," in *2012 IEEE 62nd Electronic Components and Technology Conference (ECTC), 29 May-1 June 2012*, Piscataway, NJ, USA, 2012, pp. 619-24.
- [27] A. Heryanto, W. N. Putra, A. Trigg, S. Gao, W. S. Kwon, F. X. Che, *et al.*, "Effect of Copper TSV Annealing on Via Protrusion for TSV Wafer Fabrication," *Journal of Electronic Materials*, vol. 41, pp. 2533-42, 2012.
- [28] S. E. Thompson, S. Guangyu, C. Youn Sung, and T. Nishida, "Uniaxial-process-induced strained-Si: extending the CMOS roadmap," *IEEE Transactions on Electron Devices*, vol. 53, pp. 1010-20, 05/ 2006.
- [29] M. Haouaoui, I. Karaman, K. T. Harwig, and H. J. Maier, "Microstructure evolution and mechanical behavior of bulk copper obtained by consolidation of micro- and nanopowders using equal-channel angular extrusion," *Metallurgical and Materials Transactions A*, vol. 35, pp. 2935-2949.
- [30] T. Srivatsan, B. Ravi, A. Naruka, L. Riester, S. Yoo, and T. Sudarshan, "A study of microstructure and hardness of bulk copper sample obtained by consolidating nanocrystalline powders using plasma pressure compaction," *Materials Science and Engineering: A*, vol. 311, pp. 22-27, 2001.