

**POLYLITHIC INTEGRATION OF HETEROGENEOUS MULTI-DIE
ENABLED BY COMPRESSIBLE MICROINTERCONNECTS**

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Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
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**POLYLITHIC INTEGRATION OF HETEROGENEOUS MULTI-DIE
ENABLED BY COMPRESSIBLE MICROINTERCONNECTS**

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To

my parents Myungsuk Jo and Insook Kim,

my parents-in-law Jonghwa Yun and Sookhee Jeon,

my brother Michael Jo,

and my wife and two sons Jina Youn, Ian Jo, and Ethan Jo

for their unlimited love and support.

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SUMMARY

Highly flexible and elastically deformable first-level interconnects, which we call Compressible MicroInterconnects (CMIs), are proposed and developed. The key features of the CMI technology include: 1) lithographically-defined, CMOS-compatible and batch-scale fabrication, 2) large elastic range of motion to compensate for surface non-uniformity on the attaching substrate, especially for large die or interposer assembly, and CTE mismatch induced warpage, 3) high-degree of freedom in interconnect mechanical compliance design, 4) pressure-based and non-permanent contact mechanism; since CMIs can provide temporary interconnections, they can enable chips, interposers, or packages to be replaced, hence increasing package yield, 5) no rolling effect, and 6) since thermo-compression process is not required, the assembly process is simplified as bonding parameters such as temperature may need not be considered. The CMIs, with an in-line pitch of 150 μm and height of 80 μm , are fabricated and demonstrate up to 45 μm vertical range of motion within the elastic region. Multi-height CMIs are also demonstrated with the following approximate heights of 75 μm , 55 μm , and 30 μm tall. Fine-pitch CMIs with 30 μm x 30 μm pitch and approximately 9.5 μm height are demonstrated as well.

Polyolithic integration of heterogeneous multi-die is proposed and demonstrated using a platform we call Heterogeneous Interconnect Stitching Technology (HIST). In the HIST platform, a stitch-chip with high-density fine pitch wires is placed between a substrate and chiplets. Fine-pitch interconnects are used to interconnect the chiplets to the stitch-chip to provide high-bandwidth density and low-energy signaling. CMIs are used to compensate for any possible off-chip gap differences resulting from chip thickness differences or

surface non-planarity of a substrate. HFSS RF simulation of stitch-chip links exhibit an insertion loss of less than 0.6 dB within 30 GHz and maintains good impedance matching (return loss better than -10 dB) even with the tallest CMIs (90 μm -high).

CHAPTER 1. INTRODUCTION

1.1 Current Trend of Heterogeneous Integration

In the era of Artificial Intelligence (AI), cloud computing, Internet-of-Things (IoT), big data, and autonomous computing, people are living in an increasingly digital world and are relying more on online channels for nearly every aspect of their lives. As a consequence of this reliance, the volume of data is estimated to grow to 175 zettabytes (one zettabyte is equivalent to a trillion gigabytes) by 2025, as shown in Figure 1 [1-3].

In addition to this, Cisco also predicts increasing growth of devices interconnected to the internet, and this is estimated to be more than 25 billion devices in 2022, as shown in Figure 2 [4].

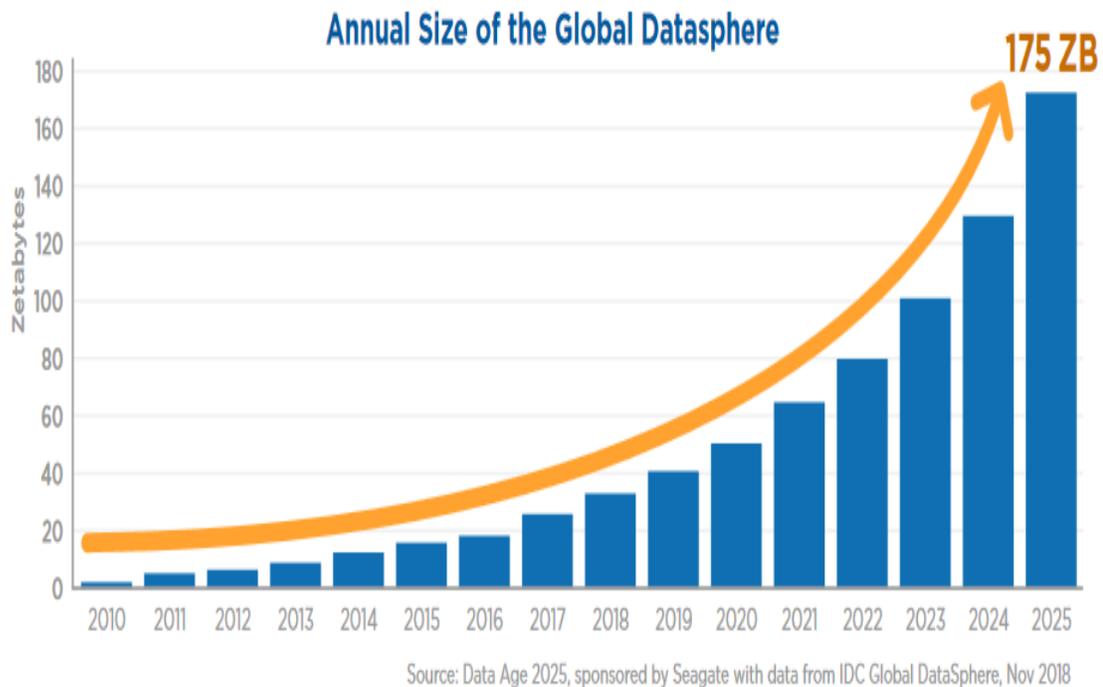


Figure 1 Annual size of the global data [1]

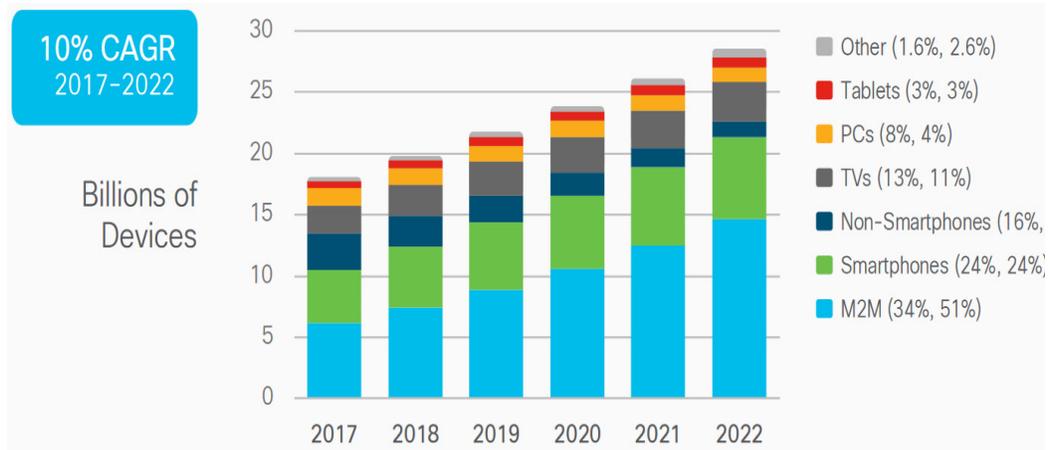


Figure 2 Global devices and connections growth [4]

This exploding growth of data and connected devices have spurred significant need in higher performance computing. This need has been fulfilled until recently by CMOS scaling as CMOS scaling brings higher computing performance and capabilities by

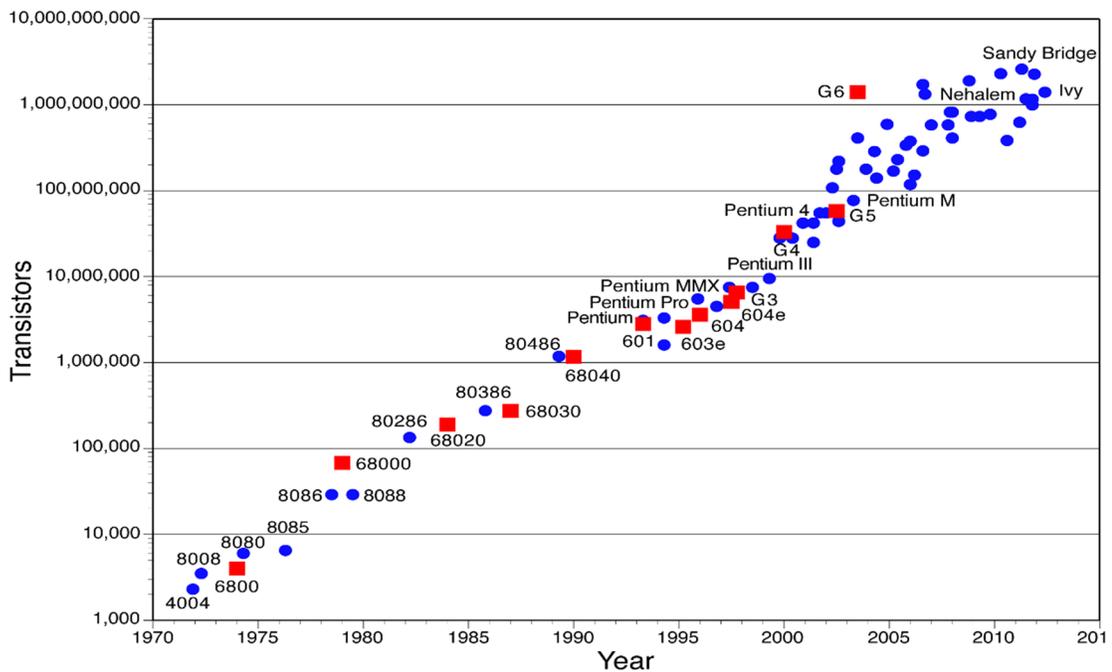


Figure 3 Microprocessor transistor counts [5]

allowing the integration of more transistors into a monolithic System-on-Chip (SoC) architecture [5], [6], as shown in Figure 3. In addition to this, performance improvement has been achieved by additional core count for both CPUs and GPUs by using larger die sizes and increasing parallelism [7]. AMD reported that the performance of GPUs and CPUs double every 2.4 years and 2.1 years, respectively, over the last 10 years through increased cores, transistor scaling, and circuit innovations. However, even though transistor scaling continues to be very important, the surging development costs and time associated with monolithic SoC designs combined with the limited materials and heterogeneous devices that can be incorporated make monolithic processes more challenging going forward [8]. In consequence, this has promoted significant research in several multi-die integration technologies by virtue of their integration flexibility and faster time to market, which has led to solutions including die stacking (3-D integration) and silicon interposer (2.5D integration). In fact, AMD reported that splitting a large die into

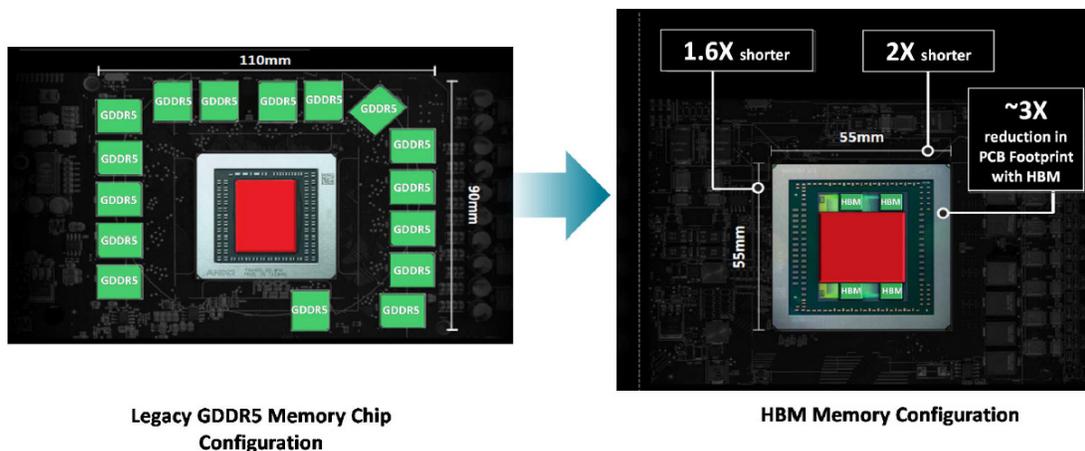


Figure 4 HBM integration brings memory closer to the processing unit and reduces overall footprint [7]

multiple smaller chiplets has the added benefits of improved overall yield and cost; AMD estimates approximately 41% cost reduction in their EPYC server chips due to the improved overall yield [7]. GLOBALFOUNDRIES reported 61% cost reduction by stacking SRAM on logic instead of monolithic integration as well [8]. Another example of system-level innovation is the use of high-bandwidth memory (HBM) integration in high-performance GPUs using 2.5-D integration technology. By shortening the distance between memory and GPU from 40 mm+ to 1 mm, as shown in Figure 4, in one example product, AMD was able to reduce the energy per bit accessed from memory by 4X [7]. In addition to this, polyolithic chiplet integration can integrate more than 200 billion transistors while monolithic integration can integrate more than 50 billion, to date, as shown in Figure 5.

Figure 6 illustrates the schematic of a typical 2.5-D and 3-D integration technology.

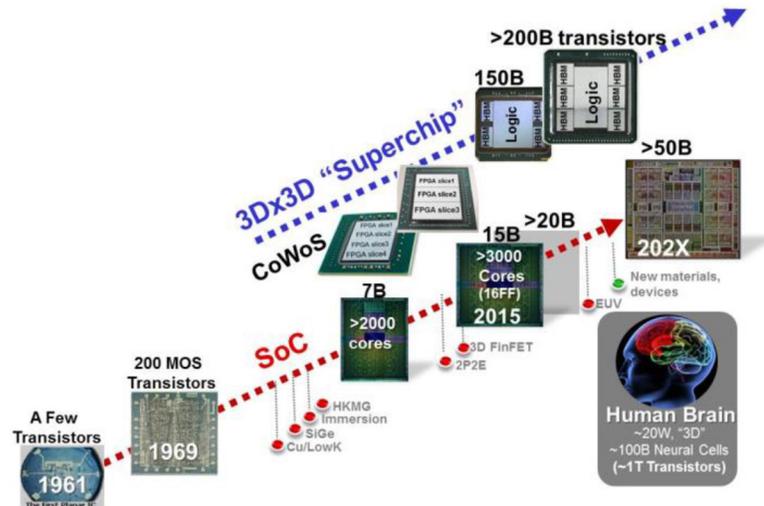


Figure 5 CMOS SoC and wafer-based 3-D x 3-D system scaling trends [5]

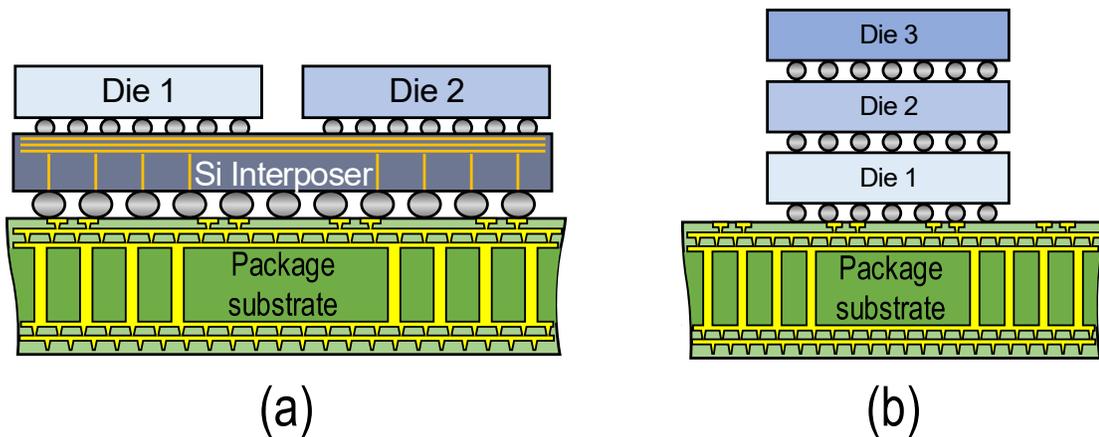


Figure 6 Schematics of typical 2.5-D and 3-D integration technology

In 2.5-D and 3-D integration technologies, interconnects are key in influencing microsystem form factor, electrical performance, power consumption, signal integrity, and a host of other system metrics. Of particular importance are first-level interconnects, which are used to electrically interconnect and mechanically bond a die to a package substrate. The density, electrical attributes, and mechanical properties of first-level interconnects impact the overall mechanical integrity of the resulting assembled microsystem, signaling bandwidth density between dice, and power supply noise in digital microsystems. While solder bumps have been widely used for first-level interconnects of 2.5-D and 3-D integration technology, they unfortunately leave a number of attributes desired in modern microsystems: 1) solder bumps are based on metallurgical bonding, and thus once they are reflowed they become irreversible, 2) solder bumps are susceptible to bump bridging, and 3) solder bumps are vulnerable to die thickness variation or surface non-planarity. The aforementioned disadvantages of solder bumps are more prevalent as pitch is scaled down.

Therefore, the research reported in this dissertation will focus on: 1) demonstration of new first-level compliant interconnects, which can possibly address the challenges that solder bumps can not address for emerging microsystems, and 2) a novel polyolithic integration technology for 2.5-D and 3-D chiplets using the compliant interconnects.

1.2 Current Technologies and Background

1.2.1 Compliant Interconnects for Emerging Electronic Devices

Compliant interconnects are vertically flexible free-standing interconnects. Their free-standing structures can absorb strain and distribute stress resulting from applied forces (deformation) within the structures, thus enabling vertical elastic motion. They can also provide some lateral flexibility by designing their structures accordingly. In addition to the mechanical flexibility, compliant interconnects can provide temporary electrical interconnection through a pressure contact mechanism, which is contrary to metallurgical bonding required for microbumps or solder bumps. Therefore, compliant interconnects can

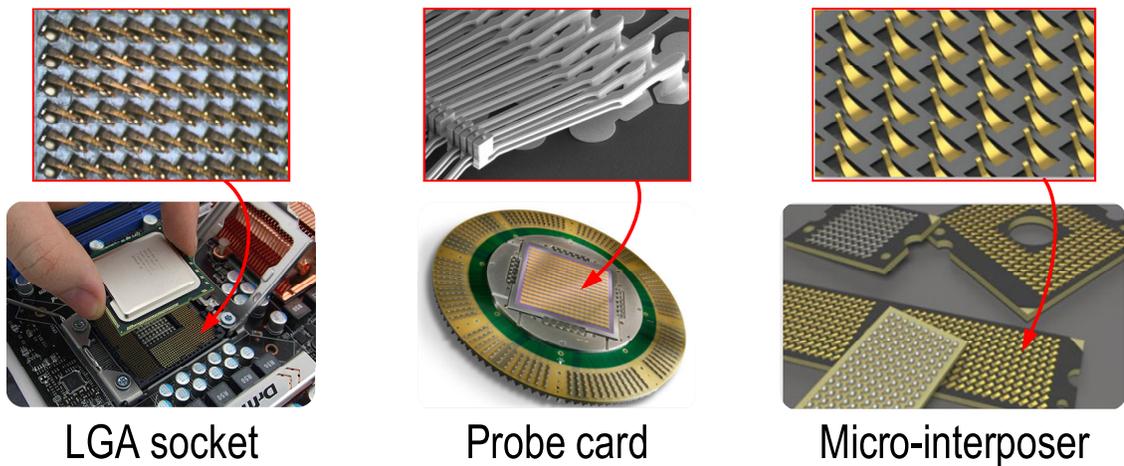


Figure 7 Applications of compliant interconnects [10], [11], [16]

circumvent many of the challenges in solder bumps as they can compensate for surface non-uniformity on the attaching substrate, coefficient of thermal expansion (CTE) mismatch induced warpage, and provide pressure-based and non-permanent contact.

Owing to these key features, compliant interconnects have been widely used in various fields, which include System-in-Package (SiP), socketed system, assembly of interposers, probe card, biosensors, etc. Figure 7 shows some of those applications using compliant interconnects. For example, as compliant interconnects can decouple the substrate and die thermal properties, accommodate for any non-uniformity from substrate and die or variation in die thickness, and provide temporary interconnections, they could potentially improve testing, rework, and thermomechanical reliability of electronic packaging [9]. Intel and AMD use compliant interconnects for their board-level socketed systems, which include Intel's Core i7 [10] and AMD's Opteron processors Land Grid Array (LGA) sockets. Since the LGA socket interconnections are pressure contact based, they allow for a simple replacement or upgrade of the interconnected processor. Moreover, compliant interconnects are vertically elastic, so they are well-suited for micro-probe tips; a micro-probe tip should be neither too stiff as to inflict damage on a pad nor too flexible so that it cannot scratch through a formed oxidation layer during probing device under test (DUT) [11, 12]. The temporary interconnections can also enable the reuse of CMOS biosensors for cell-based assays by disposing of an integrated substitutional sensing platform that sits atop the biosensor rather than the biosensor itself [13]. This reusability potentially reduces the cost of operation for bio-sensors, which are often irreversibly contaminated by blood or other cellular tissues [14, 15]. In addition to this, compliant interconnects have been used in the assembly of interposers [16].

To this end, a number of free-standing compliant interconnect technologies have been researched and presented in the literature as wafer-level interconnects; Figure 8 shows SEM images of example compliant interconnects in the literature. Microspring [17-19], Microcantilever [20], and J-Spring [21] compliant interconnects are fabricated using stress-engineered thin-film fabrication process. The stress-engineering process involves manipulating chamber pressure during metallization in order to apply very high mechanical stress gradient across metal films, which determines the radius of curvature of the released metal film. Coiled microspring [22] is also based on stress-engineering process, but it is a

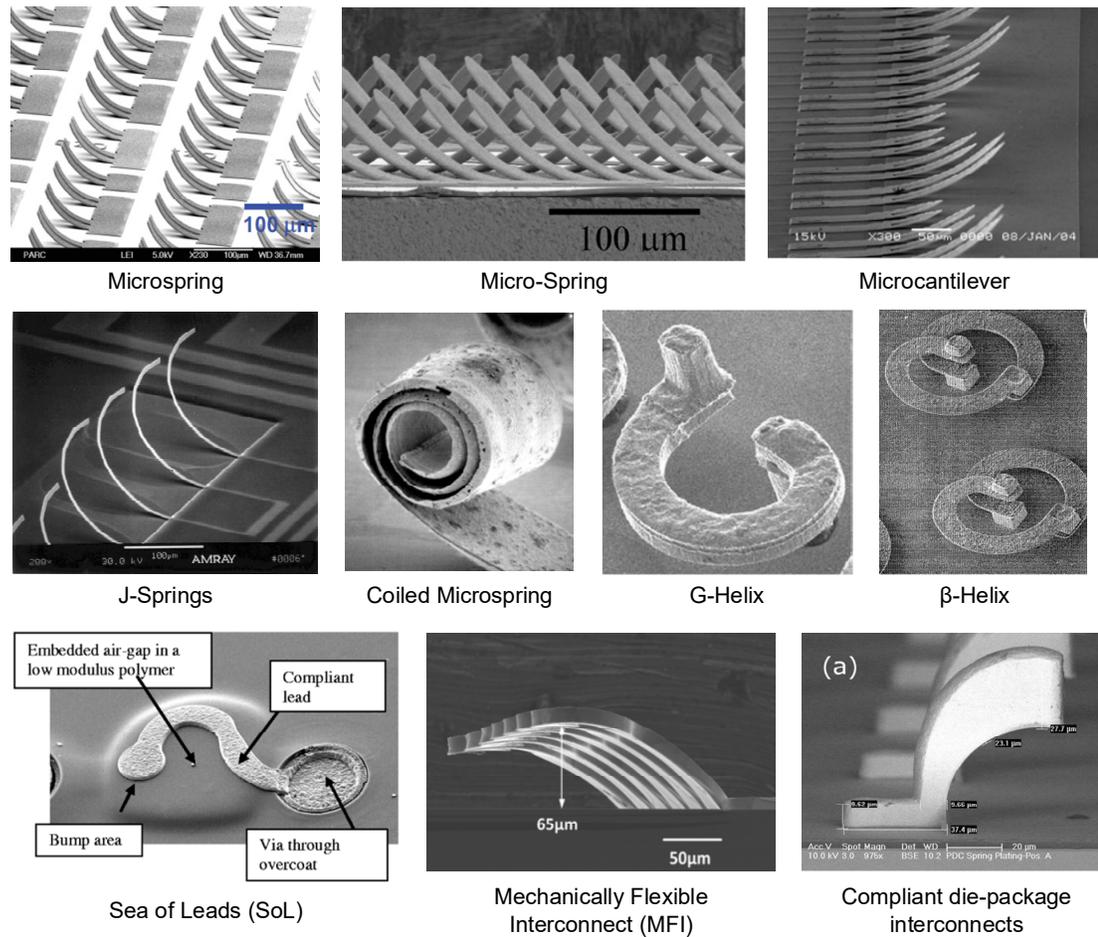


Figure 8 SEM images of various compliant interconnects

bimorph, which consists of two layers with highly different thermal expansion coefficient, so stress is created by different thermal expansion of the layers of the bimorph. G-Helix [23, 24] and β -Helix [25, 26] are a layer-by-layer electroplated interconnects. They utilize arcuate beams to enable better differential displacement in planar direction. Sea of Leads (SoL) [27, 28] utilizes embedded air gaps under the lead structures to enable high compliance. Mechanically Flexible Interconnect (MFI) [29, 30] and compliant die-package interconnect [31] are fabricated using reflowed sacrificial photoresist layer, which enables

Table 1 Comparison of published works on compliant interconnects

Reference	Pitch (μm)	Dimension (μm)	Compliance (mm/N)	Elastic range of motion (μm)	Resistance (m Ω)
Microspring [17], [18]	180	H: 45 L: 100 W: 30	167	30	72
Microspring [19]	20 (in-line)	H: 45 L: 100 W: 30	204	57	540
Microcantilever [20]	-	H: 20 ~ 260 L: 100 ~ 400 W: 50	1,493 ~ 2,500	-	1,000
J-Spring [21]	> 30 (in-line)	H: 10 ~ 50 L: 10 ~ 50 W: 10 ~ 15	> 3,500	-	-
Coiled microspring [22]	-	H: 5 ~ 35 L: 200 ~ 400 W: 40 ~ 60	0.2 ~ 10	10	-
G-Helix [23], [24]	100	H: 78 W: 13 R: 36	14.7	-	5 ~ 45
β -Helix [25], [26]	200	H: 110 R: 37	8 ~ 35	-	30 ~ 135
Sea of Leads [27], [28]	> 120	H: 60 ~ 90 L: 60 ~ 300 W: 20	0.5 ~ 2	< 35	10 ~ 50
Mechanically Flexible Interconnect [29], [30]	> 26 (in-line)	H: 50 ~ 150 L: 80 ~ 235	0.82 ~ 6.7	5 ~ 50	37 ~ 130
Compliant die-package interconnect [31]	180	H: 60~ 65	-	-	-

H: Height, L: Length, W: Width, R: Radius

spherical free-standing structures. To better differentiate the compliant interconnect technologies, a comparison is shown in Table 1.

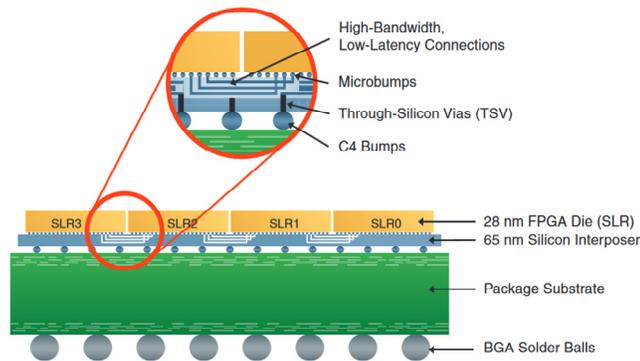
Although many compliant interconnect technologies exist, several significant issues limit their utilization in emerging microsystems. For example, while the demonstrated lithographically-defined compliant interconnects are based on simple fabrication processes, their compliance and elastic range of motion are limited [23]-[26]. Moreover, while other compliant interconnects, which are fabricated by stress-engineering, have demonstrated relatively large elastic range of motion and high compliance, they have poor controllability over their final geometric design [17]-[21]. The compliant interconnects that are used for board-level microsystems, such as LGA sockets or micro-interposers, are too big in size to be utilized in die interconnection.

To this end, a highly flexible and elastically deformable first-level interconnect, which we call Compressible MicroInterconnects (CMIs), are developed, fabricated, and characterized, and the demonstration results are reported in Chapter 2 and Chapter 3.

1.2.2 2.5-D and 3-D System-Level Integration

As discussed in section 1.1, there is a significant need for seamless integration of heterogeneous multi-die in a small footprint with high-performance interconnects. Therefore, several different system-level integration technologies have been proposed and developed by virtue of their multi-die integration flexibility, reduced costs, better electrical performance, lower energy requirement, and faster time-to-market.

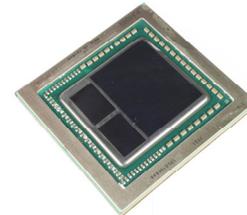
Silicon interposer, which is shown in Figure 9, is one of the representative 2.5-D integration technologies and widely used in current electronic devices. The silicon interposer is placed between chips and a package substrate, as shown in Figure 9 (a). The silicon interposer provides high-density I/Os and high signal bandwidth between the chips through fine-pitch off-chip interconnects and RDLs. Through-silicon vias (TSVs) in the silicon interposer provide power and signal interconnections between chips and the package substrate [32], [33]. Xilinx and TSMC released the first 2.5-D FPGA product



(a)



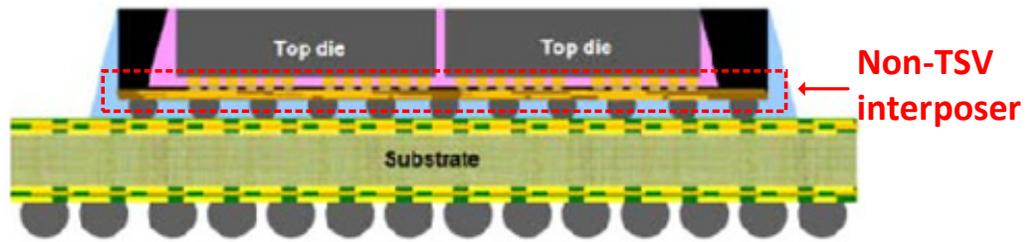
NVIDIA, Tesla P 100 GPU



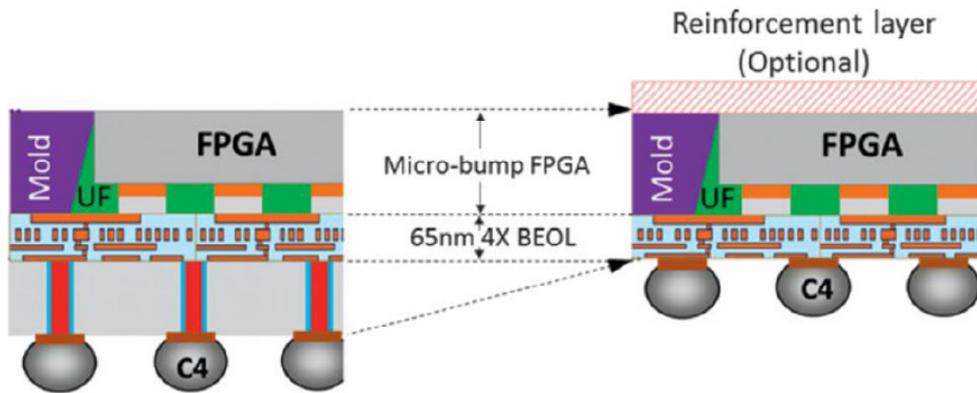
AMD, Radeon Vega Frontier Edition

(b)

Figure 9 Schematic of silicon interposer (a) and electronic devices using the silicon interposer (b) [34], [36]



(a)



(b)

Figure 10 Schematic of silicon-less interconnect technology (SLIT) (a) and comparison of SLIT and silicon interposer technology [38]

using silicon interposer [34], [35]. AMD and Nvidia have also used silicon interposer for Radeon R9 Fury X, Radeon Vega Frontier Edition, and Tesla P100 GPUs. The GPUs are supported by HBM cubes manufactured by SK Hynix and Samsung, and the GPUs and HBM cubes are assembled on top of a silicon interposer [36], [37]. In 2014, Xilinx and SPIL proposed a TSV-less interposer solution for sliced FPGA chips, which is called silicon-less interconnect technology (SLIT) [38], [39], as shown in Figure 10 (a). As shown in Figure 10 (b), TSVs and most of the silicon interposer are eliminated and only RDLs are needed for the lateral communication of the sliced FPGA chips, and thus, the RDLs are directly interconnected to C4 bumps. Recently, Intel has made a number of

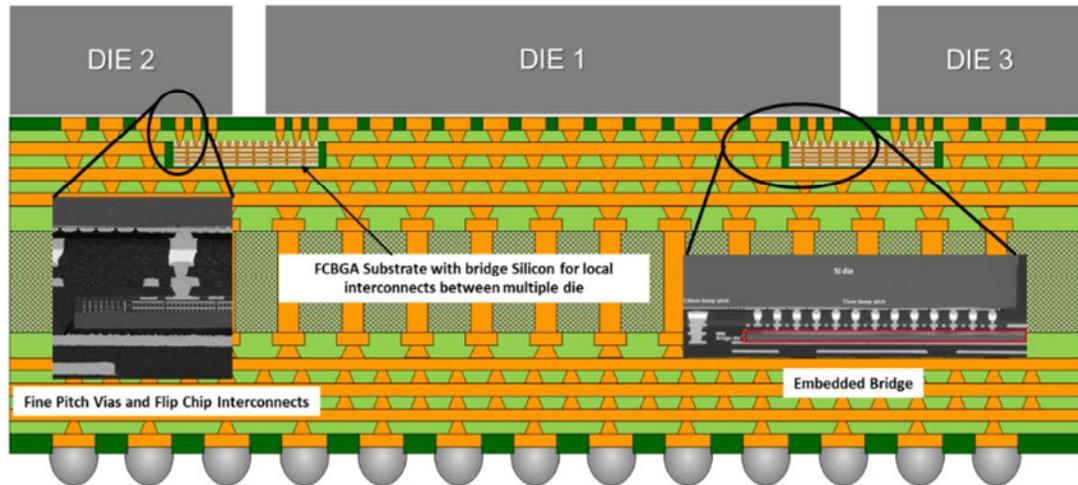


Figure 11 Schematic and SEM images of embedded multi-die interconnect bridge (EMIB) [40]

announcements concerning advanced packaging technologies. In 2016, Intel proposed a new system-level integration technology, which is called embedded multi-die interconnect bridge (EMIB) [40], [41], as shown in Figure 11. EMIB enables silicon bridges inside an organic package substrate to replace silicon interposer and provide lateral communication between chips using this technology. Intel and Altera released heterogenous packaged solutions that integrate HBM from SK Hynix with Stratix 10 FPGAs using the EMIB technology. In addition to this, Intel has formally announced the 8th generation core processors that combine Intel's CPUs and AMD's GPUs in the same package using EMIB technology. In 2018, Intel also introduced a new 3-D face-face chip stacking integration technology, called Foveros, and it is shown in Figure 12 [42], [43]. In this technology, Intel

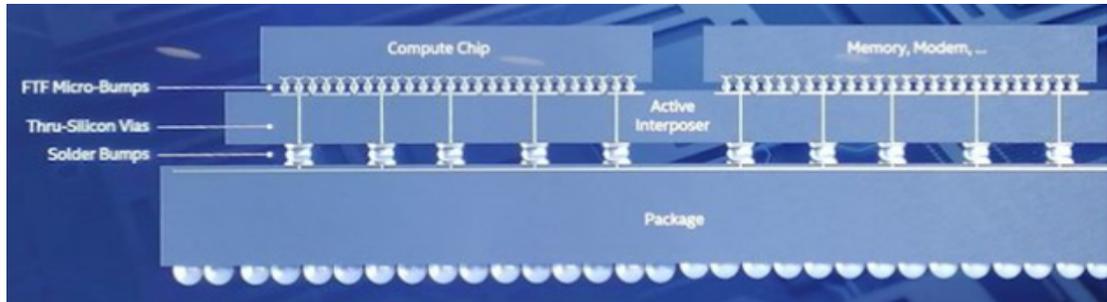


Figure 12 Schematic of Foveros technology [42]

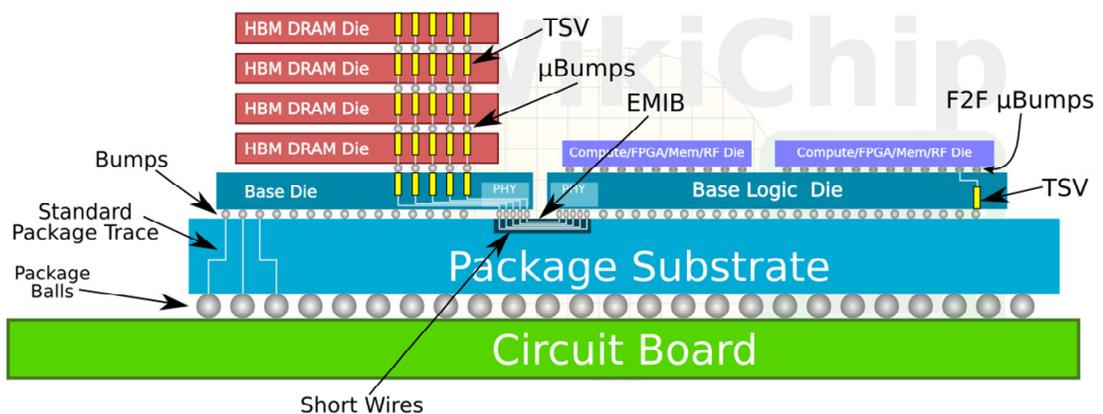
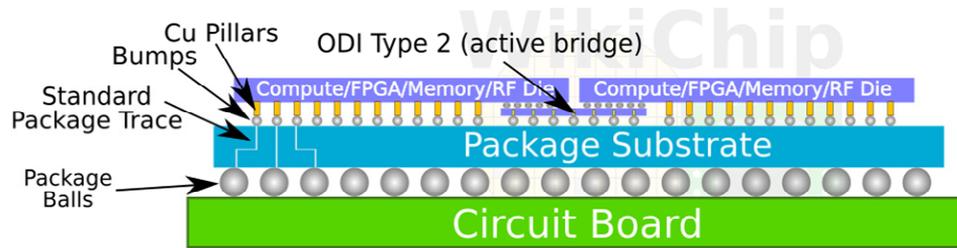
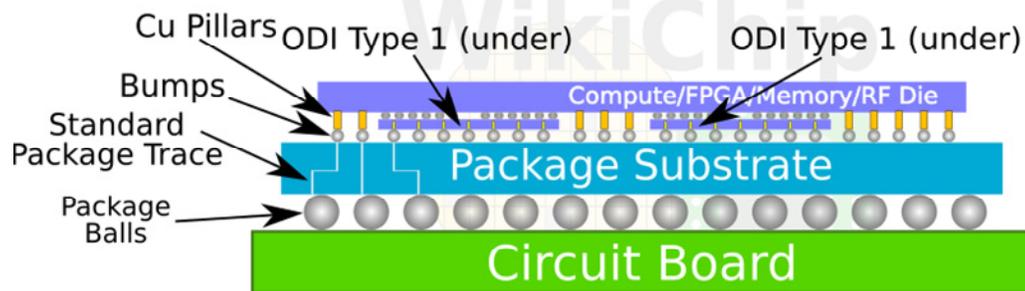


Figure 13 Schematic of Co-EMIB technology [44]

replaced a passive silicon interposer to an active TSV based interposer: the active TSV interposer is not simply an interposer with TSV and traces, but it also provides low-power components such as I/O and power delivery. Intel took the next step in 2019 to combine EMIB and Foveros into a technology called Co-EMIB, which is shown in Figure 13. In Co-EMIB technology, Intel sets up an organic package substrate with EMIB in the substrate for the dice to be assembled atop. They then take full Foveros stacks, and other dice that might be used, and attach them onto the package substrate. TSVs in the base die of the Foveros stack are exposed with fine-pitched bumps for EMIB [44]. In 2019, Intel



(a)



(b)

Figure 14 Omni-directional interconnect (ODI) [44]

also announced another new technology, which is called Omni-Directional Interconnect (ODI). As shown in Figure 14, Intel extends the idea of EMIB and chip stacking in every direction [45]. In the case of Figure 14 (a), the active bridge can provide major signal pathway between two dice, but it is not embedded in the package substrate. In the case of Figure 14 (b), active dice are fully embedded under a bigger die and have face-to-face connections with the bigger die. By using ODI technology, it can provide both horizontal (2.5-D) and vertical (3-D) integration.

While 2.5-D integration technology gives more lateral integration options for chips, 3-D integration technology provides greater vertical integration options by stacking chips in the third dimension using TSVs and microbumps [46]. The one major application that is in production using the 3-D integration technology is memory stacking with TSVs, as

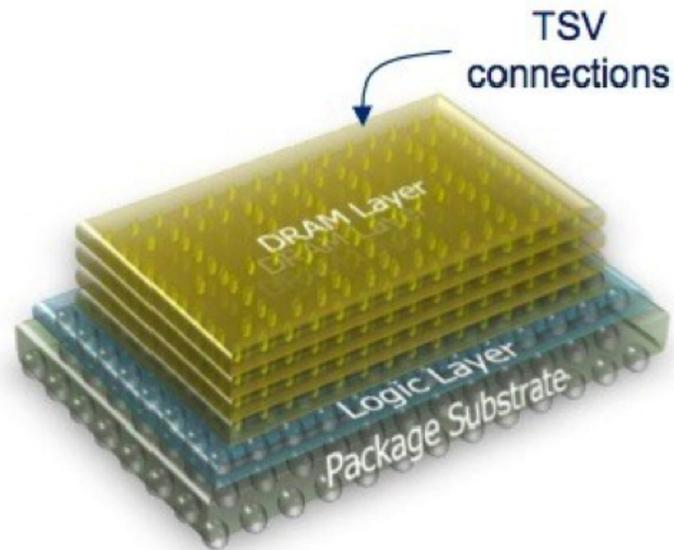


Figure 15 3-D stacked hybrid memory cube (HMC) [40]

shown in Figure 15. In 2009, Samsung announced the industry's first TSV-based DRAM stack module [47]. The module has an I/O data rate that is twice compared to typical quad-die package (QDP), while consuming approximately half the power. In 2011, Micron announced hybrid memory cube (HMC) where multiple DRAM dice are stacked on top of a logic die and interconnected with TSVs [48]. SK Hynix also developed HBM technology, which utilizes both 3-D and 2.5-D integration technologies [49]. The first product to use HBM is AMD Radeon R9 Fury X.

While the aforementioned approaches have clear advantages, they also have a number of challenges that may limit their utilization in multi-die microsystems, as shown in Table 2. For example, even though silicon interposer can provide fine-pitch interconnections, it is typically reticle size limited and requires the fabrication of TSVs, which is costly. SLIT removes the bulk silicon interposer by using a thin BEOL layer, however, the reliability of metal and dielectric layers is potentially more vulnerable to warpage by thermal cycling. Although EMIB eliminates the use of TSVs by embedding a bridge chip in an organic substrate, the organic material may potentially limit I/O density and increase parasitics. Also, the embedded silicon bridge chip in the organic substrate can

Table 2 Comparison of different system-level integration technologies

	Silicon Interposer	EMIB	SLIT	Chip stacking	Foveros	ODI
Interconnection method	2.5-D	2.5-D	2.5-D	3-D	2.5-D & 3-D	2.5-D & 3-D
I/O structure	Bumps	Bumps	Bumps	Bumps	Bumps	Bumps
Pitch	30-60 μm	55 μm	45 μm	> 7.6 μm	-	-
Requires TSV	Yes	No	No	Yes	Yes	Yes
Ability to compensate for $\Delta T/\Delta H$	Limited	Limited	Limited	-	-	-
Agnostic to package substrate	-	No	-	-	-	-
Scalability	Limited	Scalable	Limited	Scalable (Vertical)	Limited	Scalable

potentially bring reliability issues due to the coefficient of thermal expansion (CTE) mismatch between the different two materials.

To avoid the challenges, we propose an advanced TSV-less polyolithic multi-die integration technology enabled by CMIs, which we call Heterogeneous Interconnect Stitching Technology (HIST), to enable the interconnection of multi-die of various functionalities in a manner that mimics monolithic-like performance, yet provide flexibility in IC fabrication, design, and assembly. Three different types of HIST testbeds were fabricated and characterized and will be reported in Chapter 4, Chapter 5, and Chapter 6, respectively.

1.3 Organization of this Thesis

This thesis is arranged as follows:

- 1) Chapter 2: A compliant interconnect technology, which we call CMI, is developed and demonstrated. The CMIs, with an in-line pitch of 150 μm and height of 80 μm , demonstrate up to 45 μm vertical range of motion within the elastic region. In addition, electrical & mechanical characterization of the CMIs is conducted. Along with these measured characteristics, the real-time motion of CMIs during assembly is recorded to demonstrate the compliant and temporary contact between two substrates.
- 2) Chapter 3: The fabrication and characterization of fine-pitch CMIs and multi-height CMIs are presented. The fabricated multi-height CMIs are approximately 75 μm , 55 μm , and 30 μm tall, and their in-line pitch is 150 μm . Compliance and resistance of the fabricated multi-height CMIs are presented.

One of the 75 μm tall CMIs is consecutively indented for 5,000 cycles to demonstrate its mechanical reliability. The fine-pitch CMIs are formed on a 30 μm x 30 μm pitch and are approximately 9.5 μm tall and 2.5 μm thick. Down to 1 μm thick fine-pitch CMIs have been fabricated as well in order to demonstrate the wide range of compliance design. Measured compliance of the fabricated fine-pitch CMIs is verified using ANSYS FEM simulation. HFSS RF simulations are conducted to demonstrate the performance of the fine-pitch CMIs. The fine-pitch CMIs and multi-height CMIs are proposed and demonstrated to achieve dense signaling between ICs in addition to providing a highly scalable and versatile IC integration solution, which will be key enabling technologies for the proposed polyolithic multi-die integration technologies in subsequent chapters. Moreover, it is shown the multi-height CMIs can have the same mechanical compliance through geometry designs.

- 3) Chapter 4: A TSV-less polyolithic multi-die integration technology enabled by the demonstrated CMIs is proposed and demonstrated. We call the technology HIST 1.0, and it has the key features of fine-pitch (down to 10 μm x 10 μm) and 5 μm tall Au-Cu microbumps for interconnections through a stitch-chip and CMIs with 200 μm in-line pitch and 55 μm height for interconnections to a package substrate. The testbed for HIST 1.0 was fabricated, assembled, and characterized for the first time. The post-assembly electrical resistance values of the microbumps and CMIs are measured and the mechanical compliance of the CMIs is also measured. The HIST platform is proposed to achieve monolithic-like performance yet utilizes TSV-less high-density interconnection

using stitch-chips that are integrated between the chiplets and the package substrate.

- 4) Chapter 5: We advance HIST 1.0 approach and developed HIST 2.0 with fine-pitch CMIs. CMIs with 20 μm in-line pitch (instead of fine-pitch microbumps) are used to provide enhanced electrical interconnect in of HIST. Solder bumps with 50 μm height and 200 μm x 200 μm pitch are used for power delivery, signal routing between a die and package, and mechanical interconnection between anchor chips and a package substrate. The testbed for HIST 2.0 was fabricated, assembled, and characterized. In addition, chips containing fine-pitch CMIs were flip-chip bonded onto three substrates containing different stitch-chip thickness mismatches to demonstrate the flexibility of CMIs for stitch-chip thickness variation or surface non-planarity of a substrate. Post assembly four-point resistance measurement results for both solder bumps and fine-pitch CMIs show a robust signal routing between two anchor dice through stitch-chips with low resistance variation. These results demonstrate a superior mechanical advantage when compared to conventional microbumps; moreover, they enable assembly on non-planar surface.
- 5) Chapter 6: A polyolithic integration technology (HIST 3.0) enabled by multi-height CMIs is proposed and demonstrated. We replaced all off-chip interconnects with fine-pitch and multi-height CMIs to enable replaceability of dice easily. Since the CMIs are elastically compressible unlike conventional solder bumps, the proposed polyolithic integration technology can compensate for any possible off-chip interconnection distance differences resulting from

chip thickness differences; this can enable both 2.5-D and 3-D face-to-face interconnection in one platform. Experimental characterization of the proposed approach was performed by assembling a testbed using multi-height CMIs and surface-embedded chips emulated using a silicon step. We also present HFSS-based simulations of the CMIs and stitch-chips to gain initial insight into their high-frequency response. This HIST platform, which utilizes multi-height CMIs, enables the ultimate flexibility in heterogeneous integration.

CHAPTER 2. COMPRESSIBLE MICROINTERCONNECTS (CMIS)

As discussed in Section 1.2.1, a number of free-standing compliant interconnect technologies have been presented in the literature. Although many compliant interconnect technologies exist, several significant issues limit their utilization in emerging microsystems. For example, while the demonstrated compliant interconnects [23-25] are based on simple and lithography based fabrication processes, their compliance and elastic range of motion are limited. Also, while stress-engineering technology is used for fabricating upward-curved interconnects [17-21], they have poor controllability over their final geometric design. The compliant interconnects for board-level systems, including LGA sockets or micro-interposers, are typically few millimeters (mm) tall, so they are too large in size to be utilized for die interconnection.

To this end, we develop a highly flexible and elastically deformable first-level interconnect, which we call Compressible MicroInterconnects (CMIs). The key features of the CMI technology include: 1) lithographically-defined, CMOS-compatible and batch-scale fabrication, 2) large elastic range of motion to compensate for surface non-uniformity on the attaching substrate, especially for large die or interposer assembly, and CTE mismatch induced warpage, 3) high-degree of freedom in interconnect design, 4) pressure-based and non-permanent contact mechanism; since CMIs can provide temporary interconnections, they can enable chips, interposers, or packages to be replaced, hence increasing package yield, 5) no rolling effect, as shown in Figure 16, and 6) since thermo-compression process is not required, the assembly process is simplified as bonding parameters such as temperature may need not be considered [50]. With the aforementioned key features, the CMI technology can be a key enabler for seamless integration of

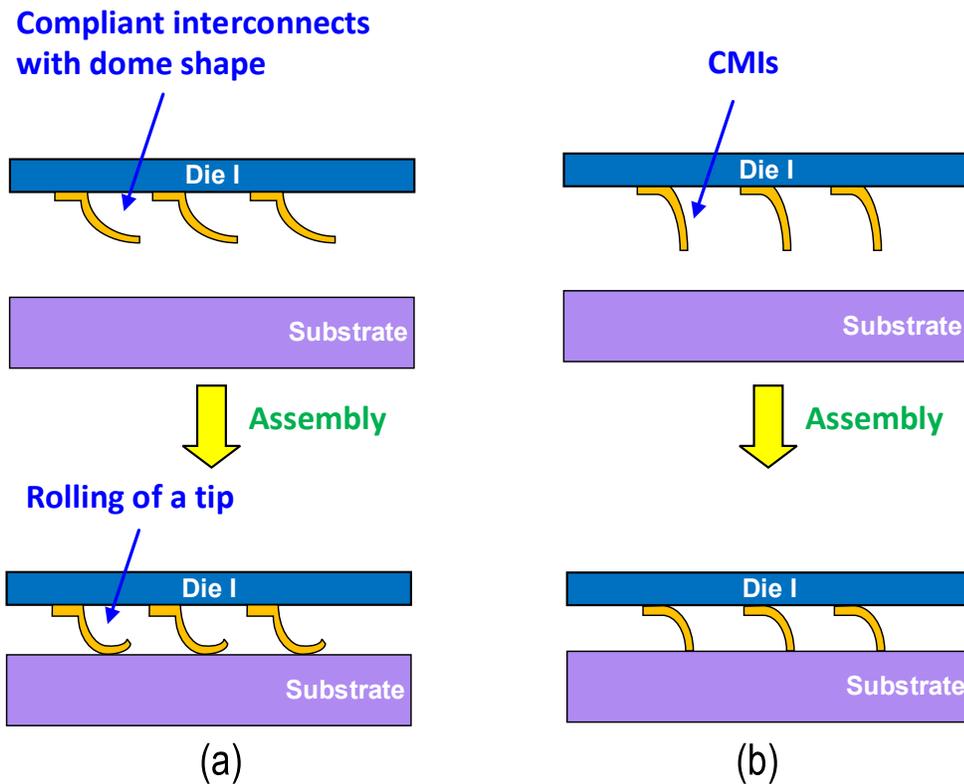
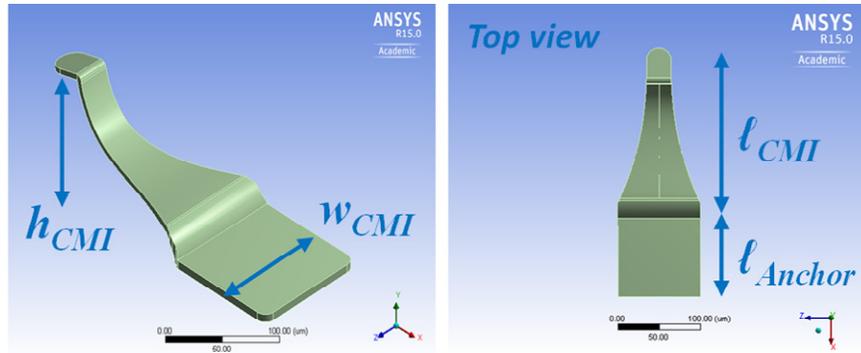


Figure 16 (a) Rolling effect of compliant interconnects with dome shape and (b) CMIs without rolling effect

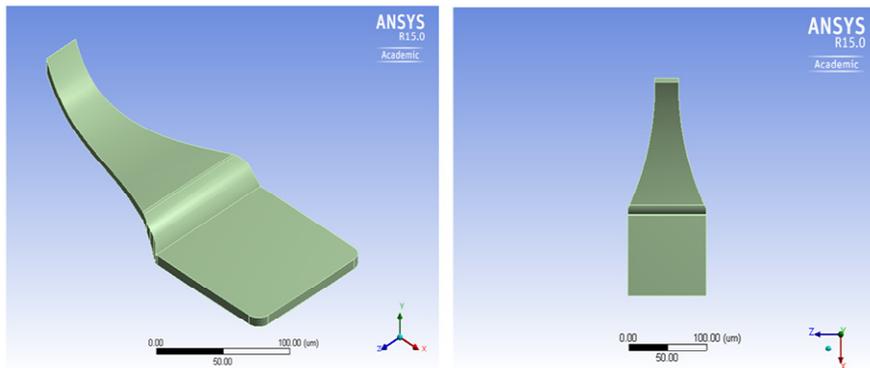
heterogeneous systems while offering design versatility and replaceability for next-generation microelectronic applications.

2.1 Design of CMIs

Since CMIs are lithographically defined and agnostic to substrate material (compatible with glass, ceramic, FR4, etc.), many different interconnect designs can be explored. For example, the tips of the CMIs can be designed such that the contact region between the CMI tip and the corresponding contact pad is controlled and hence, the contact



(a)



(b)

Figure 17 ANSYS FEM simulation geometry of the CMI with a platform-like tip (a) and with a single line tip (b)

resistance is effectively modified. The sizes and shapes of these contact regions can be adjusted, via the CMI tip. For example, a CMI that is designed to have a platform-like tip, as shown in Figure 17 (a), may form a large contact area onto the mating pad; the CMI in this example possesses $80\ \mu\text{m}$ of vertical height (h_{CMI}) and $190\ \mu\text{m}$ of length (l_{CMI}) from the junction of the anchor to the tip. Alternatively, a CMI with a ‘blunt’ tip is shown in Figure 17 (b), which forms a line contact with the mating pad. The shown CMI is approximately $75\ \mu\text{m}$ in height (h_{CMI}) and $150\ \mu\text{m}$ in length (l_{CMI}). Both CMI designs have

Table 3 Specifications of CMIs

	h_{CMI}	ℓ_{CMI}	ℓ_{Anchor}	w_{CMI}
CMI for large area contact	80 μm	190 μm	100 μm	100 μm
CMI for single line contact	75 μm	150 μm	100 μm	100 μm

a square anchor of 100 μm length (ℓ_{Anchor}) and 100 μm width (w_{CMI}). The geometric specifications of the CMIs are summarized in Table 3.

In order to maximize the vertical elastic range of motion, CMIs with an approximate tapered design are implemented in an effort to uniformly distribute the stresses during deflection [51]. In addition, CMIs were fabricated using NiW to enhance this mechanical advantage and to be more durable under stress (relative to copper) [52]. Specifically, NiW can achieve a yield strength of 1.93 GPa, whereas Cu has a yield strength of 136 MPa [53]. Therefore, compared to Cu, NiW enables the CMI to withstand higher stress before experiencing plastic deformation, which would cause permanent change to the geometric profile of the CMI and thus may exacerbate interconnect reliability. Even though Cu has better electrical characteristics than that of NiW, it is the mechanical performance of the compliant interconnect that we wish to exploit, hence NiW has been used; electroless gold plating is used to passivate the CMI to prevent oxidation which helps to lower contact resistance [31]. The CMI has a vertically curved-up geometry (or convex profile with respect to the substrate on which they are fabricated on), and this ensures that the contact region formed during deflection remains on the tip of the CMI. To date, stress-engineering has been employed to fabricate such upward-curved interconnects, which limits its application space significantly due to its less-than needed controllability in obtaining targeted geometric specifications which may be problematic when undergoing batch fabrication. Moreover, difficulty in achieving targeted geometric specifications

contributes to difficulty in achieving certain mechanical (and electrical) characteristics such as a specified compliance. However, we demonstrate, for the first time, the fabrication of upward-curved compliant interconnects utilizing a lithographic process, which is not only simpler but allows for more versatility in design (more geometries, materials, etc.) relative to stress-engineering, as will be shown in the next section.

The CMI was modeled using ANSYS finite element method (FEM), as shown in Figure 18. For the simulations, Static Structural analysis system was used, and NiW material was used to form the CMI model. Young's modulus and Poisson's ratio of the NiW material is 1.8×10^{11} Pa and 0.3, respectively. Both Cu- and NiW-based CMIs were deformed to a vertical depth of $45 \mu\text{m}$ in the simulation. Table 4 summarizes the parameters for the ANSYS simulation. The simulation results show that the maximum von Mises stress

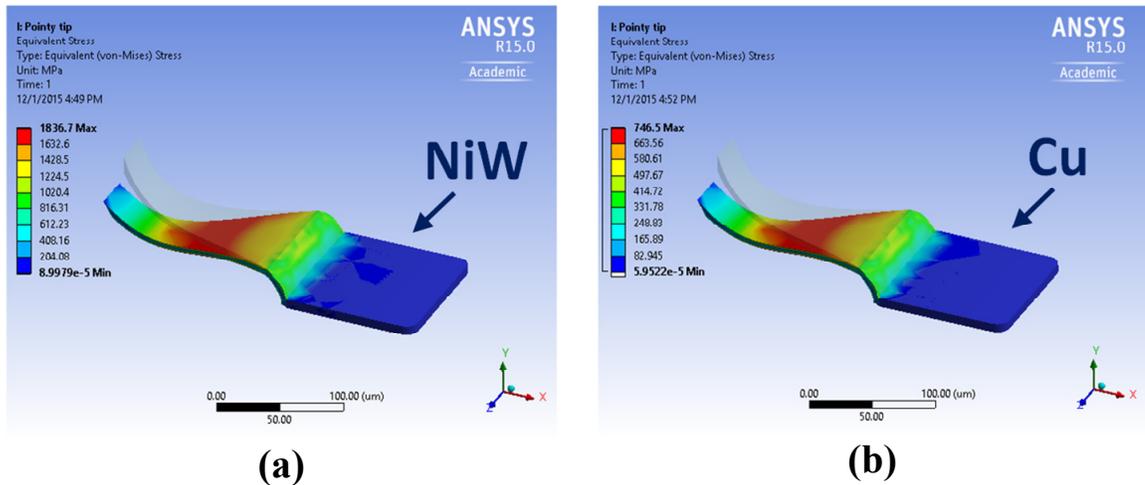


Figure 18 ANSYS FEM indentation simulation of the CMI with NiW (a) and Cu (b)

Table 4 ANSYS FEM simulation setup

Analysis system	Static Structural	
Remote displacement	Y-axis: 45 μm (vertical deformation)	
CMI geometry	Height	75 μm
	Thickness	7.6 μm and 10.5 μm
	CMI body length	150 μm
	CMI anchor length	100 μm
	CMI anchor width	100 μm
CMI material	Material	NiW
	Young's modulus	1.8×10^{11} Pa
	Poisson's ratio	0.3
	Bulk modulus	1.5×10^{11} Pa
	Shear modulus	6.9231×10^{10} Pa

for the NiW CMI is approximately 1.83 GPa for the 45 μm vertical deformation, which is less than the yield strength of NiW (1.93 GPa) [52]. However, the maximum von Mises stress for the Cu CMI is approximately 746 MPa, which is larger than the yield strength of Cu (136 MPa), and hence plastic deformation is experienced by the Cu CMI. Thus, the mechanical characteristics of the NiW CMI ensure that the CMI does not undergo permanent plastic deformation and can return to its original position despite its large vertical deflection, which is 60% of its total height in this case.

2.2 Fabrication Process

The overall fabrication process of CMIs is illustrated in Figure 19. The first step is the spin coating of a sacrificial photoresist layer (AZ 40XT-11D) onto the surface of the wafer followed by patterning the sacrificial photoresist to exhibit a curved sidewall profile. Figure 20 shows the microscope top-view image of the patterned sacrificial photoresist layer and their cross-sectional profile. As shown in the profile, the sacrificial photoresist layer has a upward curved sidewall. Next, a Ti/Cu/Ti seed layer is deposited followed by spray coating photoresist (AZ P4620) to form the electroplating molds.

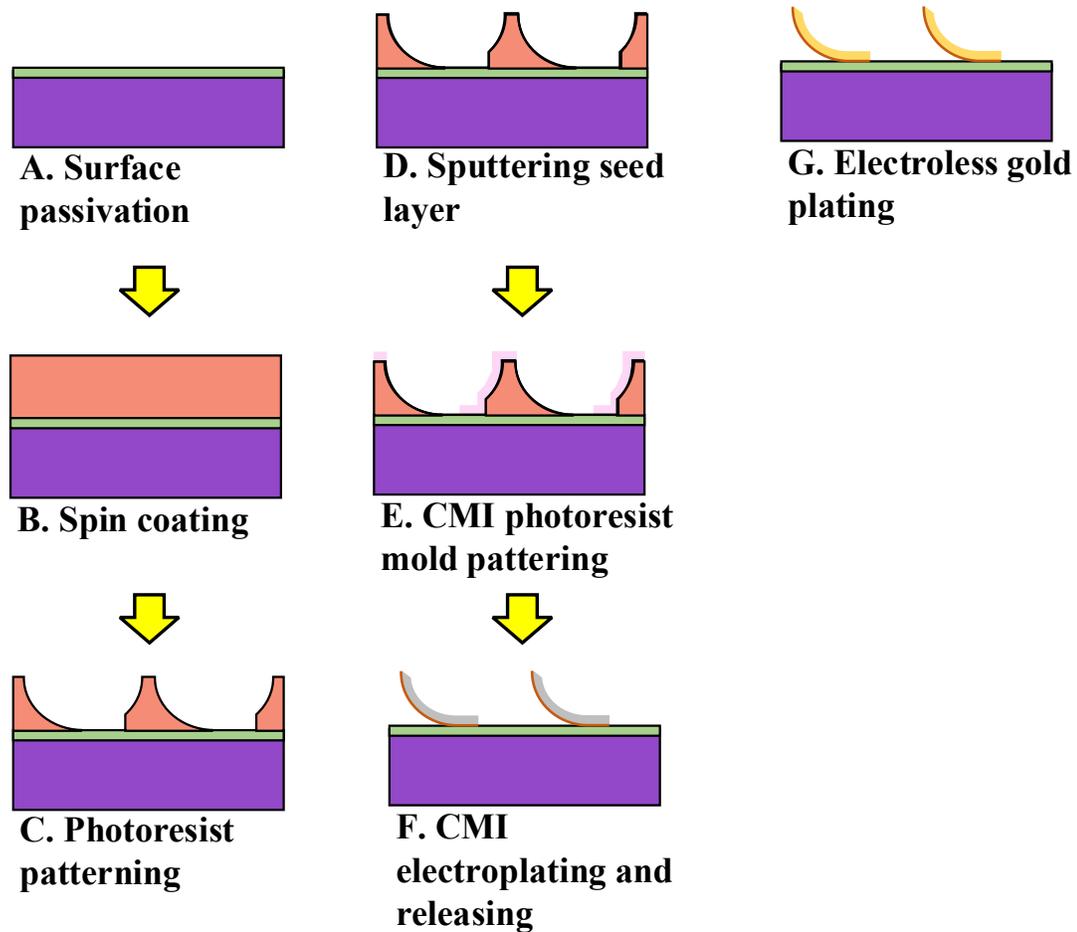


Figure 19 Fabrication of CMIs

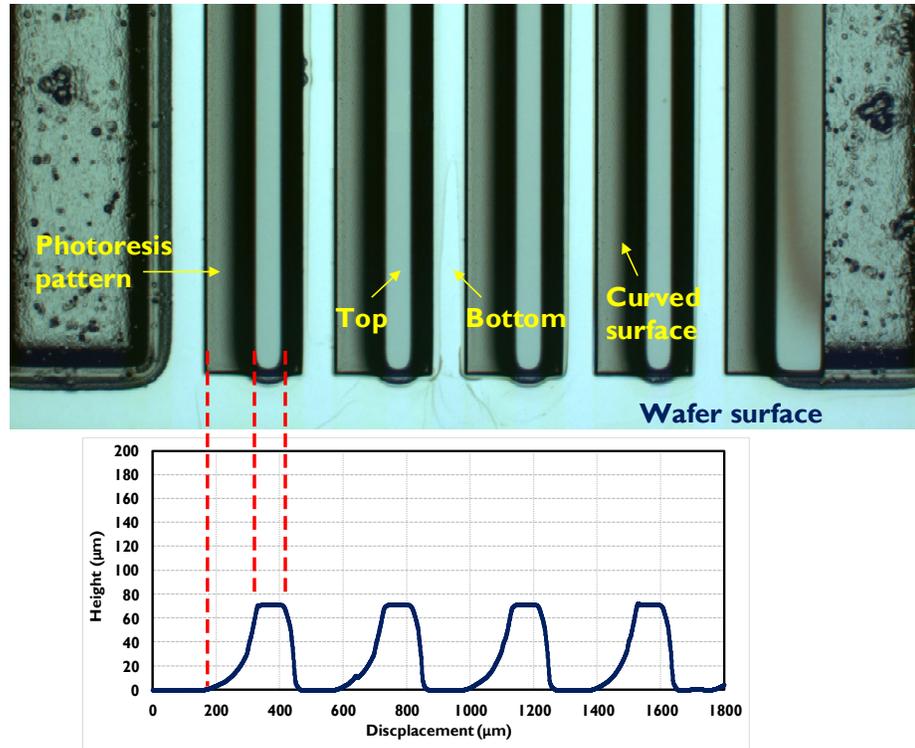


Figure 20 Microscope image of the patterned sacrificial photoresist layer and their measured cross-sectional profile

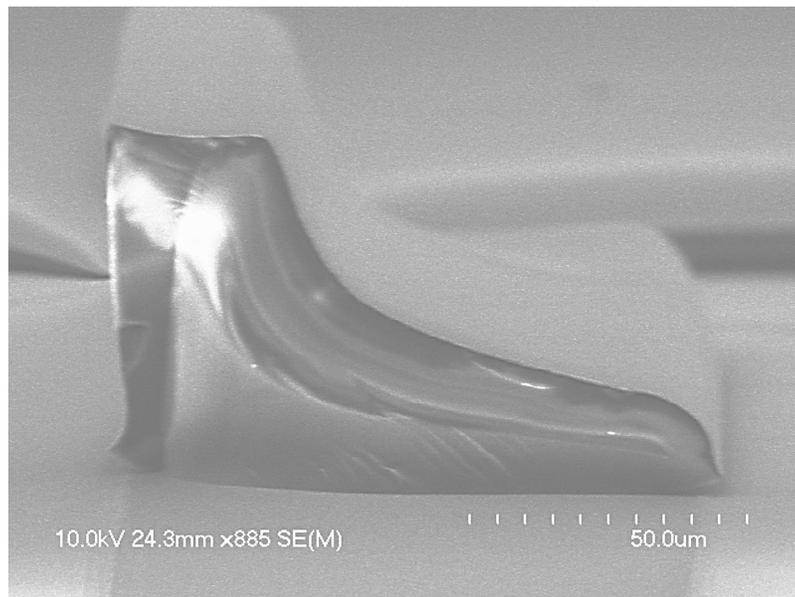


Figure 21 Cross-sectional SEM image of the patterned sacrificial photoresist layer after Ti/Cu/Ti seed layer deposition

Figure 21 shows the cross-sectional SEM image of the sacrificial photoresist layer after the seed layer deposition, and Figure 22 shows the microscope image of CMI electroplating molds in the spray coated photoresist layer. During electroplating, NiW is deposited within the mold to form the CMIs. After electroplating, the mold photoresist layer, the Ti/Cu/Ti seed layer, and the sacrificial photoresist layer are removed in sequence leaving behind free-standing CMIs. Finally, the CMIs are passivated by electroless gold plating in order to prevent the oxidation of NiW, which negatively affects the mechanical and electrical characteristics. CMIs are immersed in gold electroless plating solution such that all exposed CMI surfaces are coated with gold [30]. In order to investigate the differences in mechanical and electrical properties as a function of thickness, two samples of different thicknesses ($7.6\ \mu\text{m}$ and $10.5\ \mu\text{m}$) are fabricated. Figure 23 and Figure 24 show the SEM images of the fabricated CMIs. Measurements are reported in the next section.

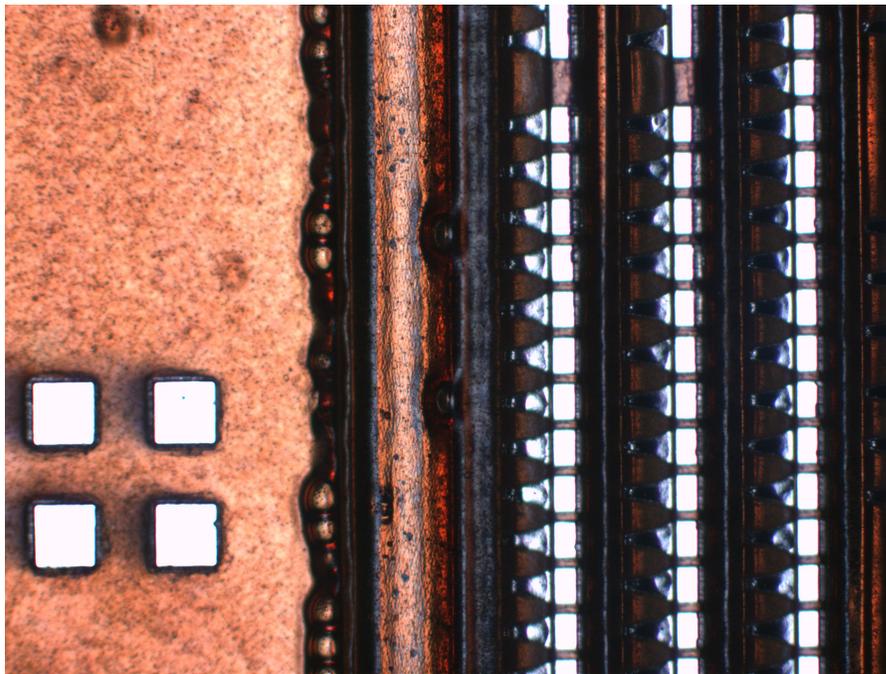


Figure 22 Microscope image of CMI electroplating molds

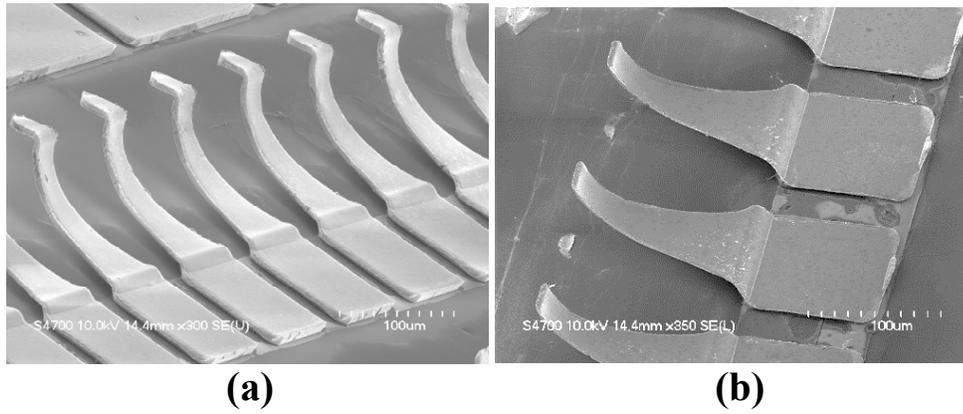


Figure 23 SEM images of the CMI with the platform-like tip (a) and line at the tip (b)

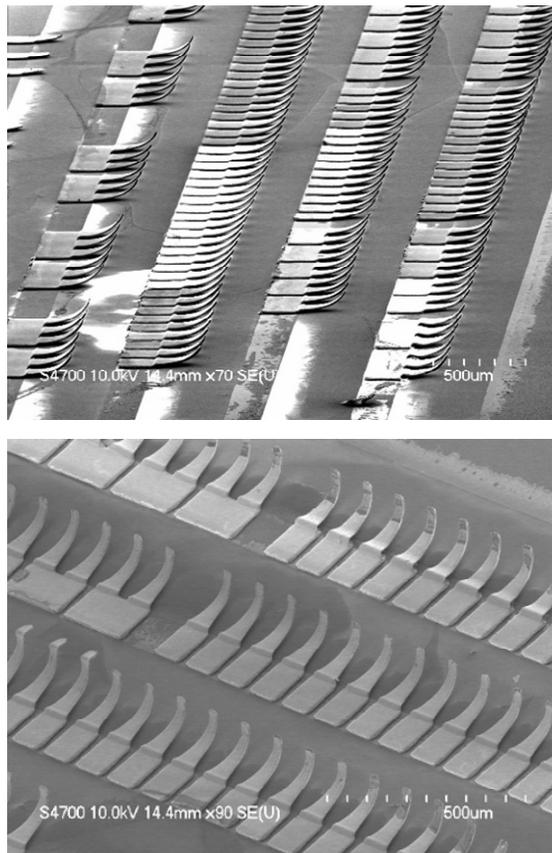


Figure 24 SEM images of an CMI array

2.3 Mechanical and Electrical Characterization

A chip containing 336 CMIs was batch fabricated (Figure 25 (a)) and flip-chip bonded onto a silicon substrate containing gold pads on its surface for four-point resistance measurements (Figure 25 (b)). Ti/Cu/Au seed layer was deposited using evaporator, in order to make the pads. After aligning and lowering the chip into contact with the substrate, epoxy was applied to each of the four chip corners to hold the chip onto the test substrate, as shown in Figure 25 (c), to facilitate measurements. In order to check the alignment between the CMIs and pads after flip-chip bonding, X-ray imaging was performed using a Dage X-Ray XD7600NT revealing accurate alignment. In order to investigate the real-time motion of the CMIs during deformation, a cross section of the assembled chip was recorded before the epoxy was applied using a Keyence VHX-600 Digital Microscope. Figure 26 shows the motion of a single CMI when the applied force increases, and thus, the gap between the chip and substrate is decreased. Even after several instances of deformation, the CMI returns to its original position, which is indicative of elastic behavior. This also

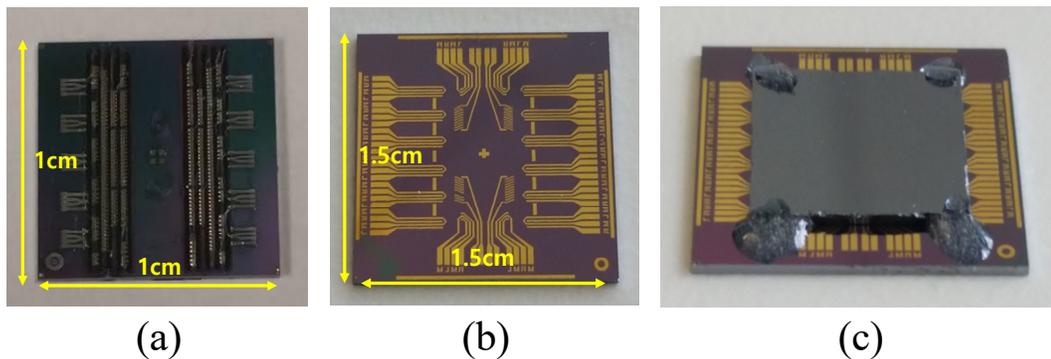


Figure 25 336 CMIs were batch fabricated on a chip (a) and then flip-chip bonded with the test substrate (b). The chip was bonded by applying epoxy (c)

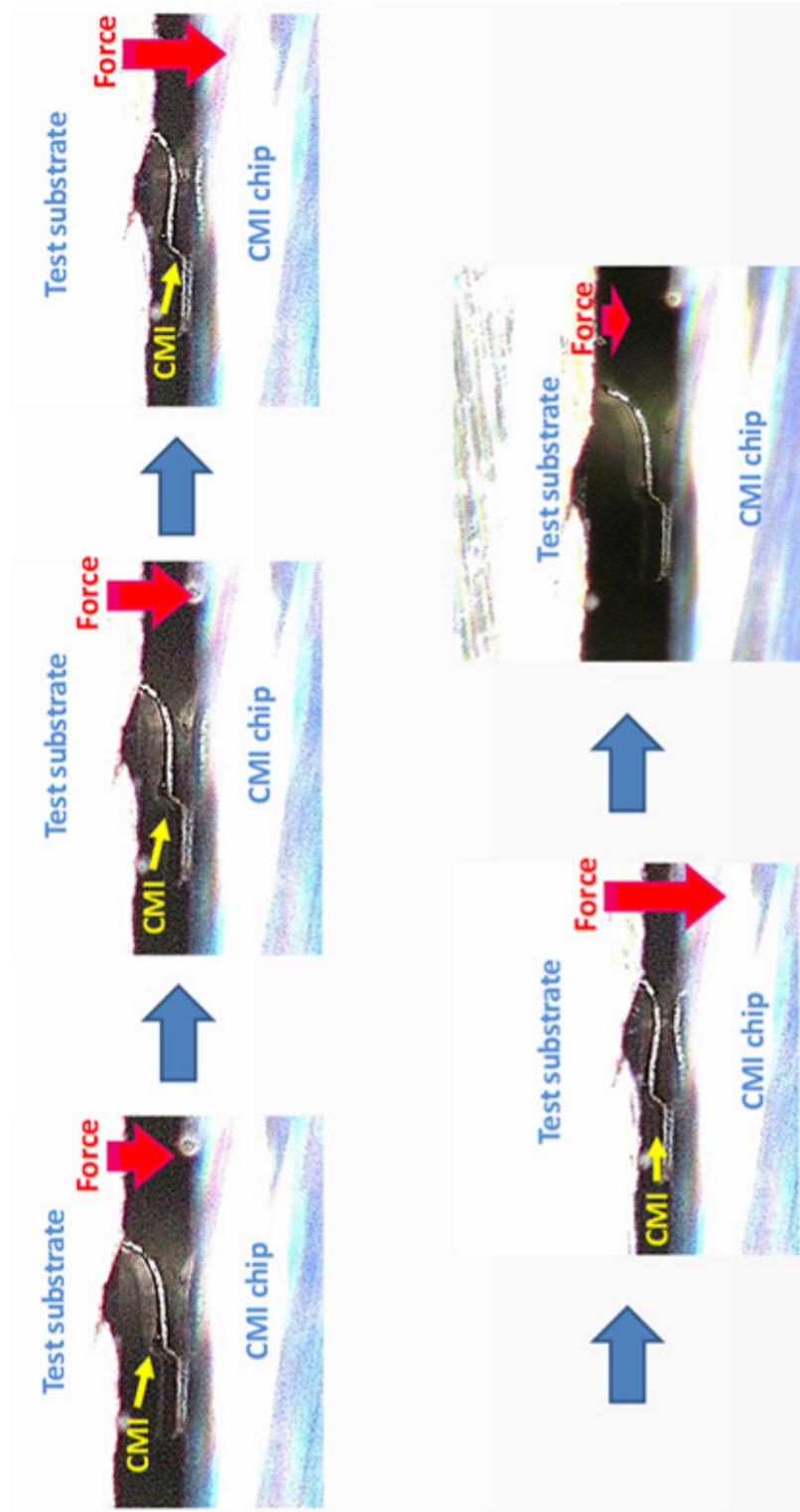


Figure 26 Cross-section view of the assembled chip while applying force from the top substrate. It is shown that CMIs are bending with respect to force

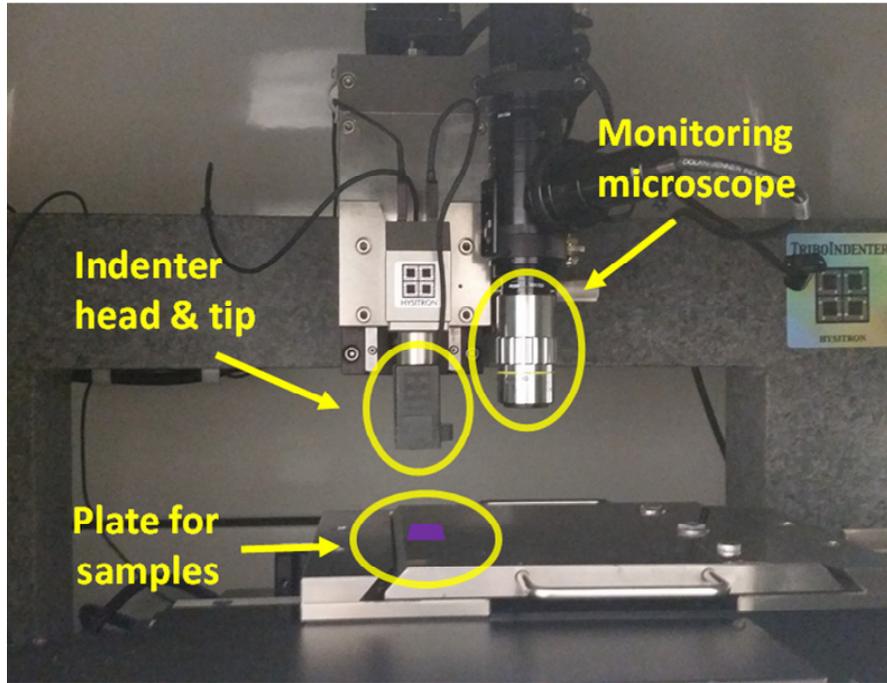
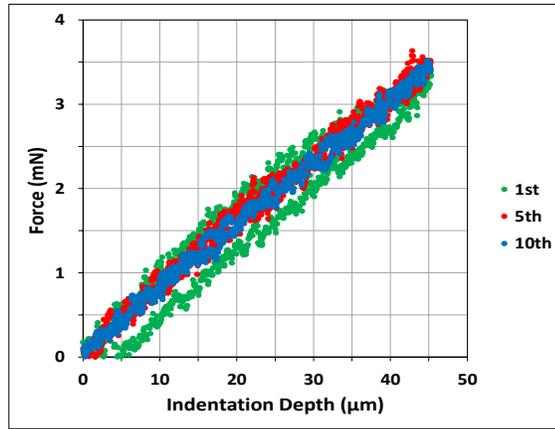


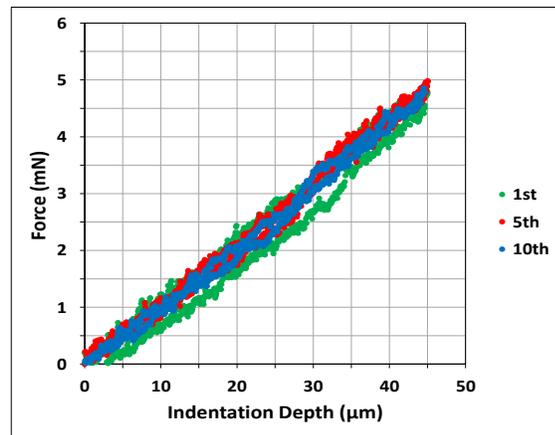
Figure 27 Compliance measurement using Hysitron Triboindenter

demonstrates that the CMI maintains electrical contact with the pad via its tip during deflection.

Compliance, which is the inverse of stiffness, is a key property of flexible interconnects since it is related to the ease of the vertical motion within the elastic region during the assembly process. Hysitron Triboindenter with a Cono-Spherical probe tip was used to measure the compliance of CMIs, as shown in Figure 27. Compliance of the CMI was measured by positioning the Cono-Spherical probe tip directly on the top flat area of the CMI; this was done for both CMI thickness values of $7.6\ \mu\text{m}$ and $10.5\ \mu\text{m}$. In each indentation cycle, there are two steps: a downward moving step and an upward moving step. During the downward motion of indentation, the CMI is deformed downward by the probe tip to a preset depth, and the applied force versus displacement data of the CMI is



(a)



(b)

Figure 28 Force versus indentation depth curve of CMI with (a) 7.6 μm and (b) 10.5 μm thickness

recorded. In the same way, the reaction force of the CMI on the probe while it recovers to its original position is recorded during the upward motion of indentation. The CMI was deflected downward by 45 μm , and the indentation test was repeated 10 times on the same CMI to confirm repeatability. The results of the indentation tests are shown in Figure 28. Figure 28 (a) is the force versus indentation depth graph of the 7.6 μm thick CMI, and Figure 28 (b) is that of the 10.5 μm thick CMI. As seen in Figure 28, the initial indentation

Table 5 Compliance data from simulation and measurement

		Thickness	
		7.6 μm	10.5 μm
Compliance (mm/N)	Simulation	12.9	7.3
	Indentation measurement	13.12	9.34

shows some minor plastic deformation. However, the CMI undergoes elastic recovery and hence all subsequent indentations are able to attain up to 45 μm of vertical elastic deformation and continue to do so even after several deflection cycles: the indentation induces work hardening of the structure and introduces defects into metal, causing an increase in the yield strength for subsequent indentations [75]. The compliance data from the measurements and simulations are shown in Table 5. The compliance of the 7.6 μm and 10.5 μm thick CMIs is 13.12 mm/N and 9.34 mm/N, respectively. Similar compliance data was obtained for the tested CMIs using ANSYS FEM simulations of Figure 18.

The electrical resistance of the CMIs with a ‘blunt tip’ (line contact) was measured by performing a four-point resistance measurement with a Signatone probe station. The

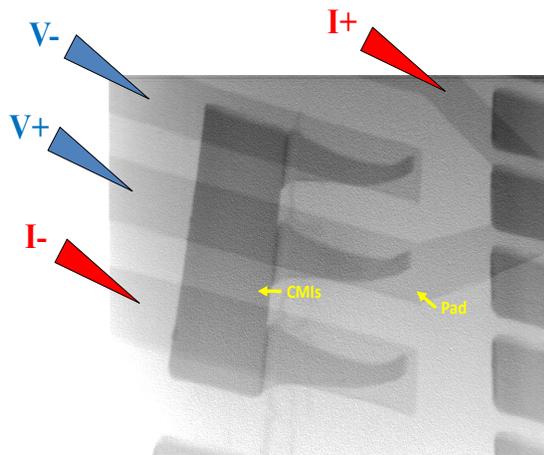


Figure 29 CMI structure for four-point resistance measurement

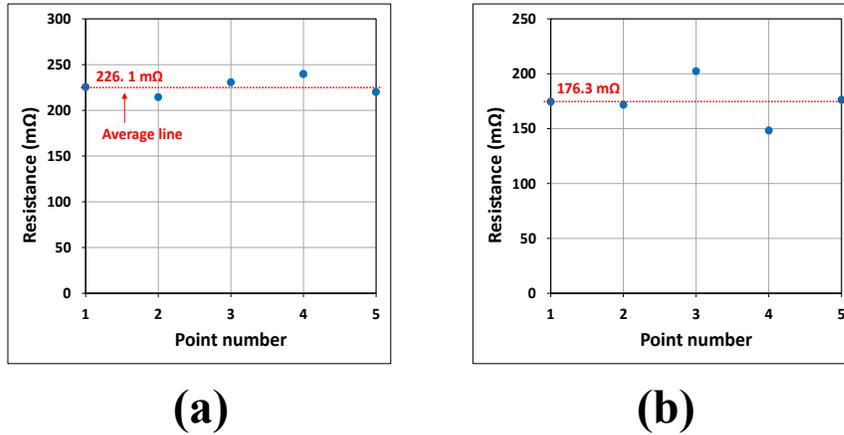


Figure 30 Four-point resistance of CMIs with (a) 7.6 μm thickness and (b) 10.5 μm thickness

Table 6 Resistance data from measurement

		Thickness	
		7.6 μm	10.5 μm
Resistance (mΩ)	Average four-point resistance	226.1	176.3

CMI four-point resistance structure, which consists of three CMI bodies sharing a single anchor, as shown in Figure 29, was used to measure the CMI four-point resistance. Since the CMI chip and the test substrate are flip-chip bonded, CMIs are partially bent and thereby the tips of the CMIs remain in contact with the corresponding mating pads. By applying a current source and using a voltmeter on the appropriate contact pads, resistance data, which includes the resistance of the CMI and the contact resistance, can be measured. The results are summarized in Figure 30 and Table 6. The average four-point resistance of the 7.6 μm thick CMIs is 226.1 mΩ and that of the 10.5 μm thick CMIs is 176.3 mΩ.

2.4 Conclusion

In this chapter, highly flexible NiW CMIs are batch fabricated using standard CMOS-compatible processes. The CMIs, with an in-line pitch of 150 μm , demonstrate up to 45 μm vertical range of motion within the elastic region. In addition, the CMIs show favorable mechanical and electrical characteristics; the measured compliance of the fabricated CMIs is as high as 13.12 mm/N, while the four-point resistance, including contact resistance, is as low as 176.3 m Ω . Along with these measured characteristics, the real-time motion of CMIs during bonding demonstrates the compliant and temporary contact between two substrates. Since CMIs are lithographically defined, they can easily keep pace with I/O pad size and pitch reduction. Lastly, the high degree of freedom in interconnect design enables CMIs to be easily engineered, and therefore this can enable CMIs to be used in various applications.

CHAPTER 3. MULTI-HEIGHT AND FINE-PITCH COMPRESSIBLE MICROINTERCONNECT (CMI)

There is an ever growing need for higher I/O densities to meet increasing signal bandwidth requirements for high-performance computing systems. Many different system-level integration technologies have been introduced to enable high-speed and high-bandwidth density communication between dice and new architectures continue to demand scaling of off-chip interconnections with pitches projected to reach down to 10 μm [76] and probably less, as shown in Figure 31. In addition to this, TSMC also introduced sub-micron pitch Au-Au direct bonding for future high performance computing application

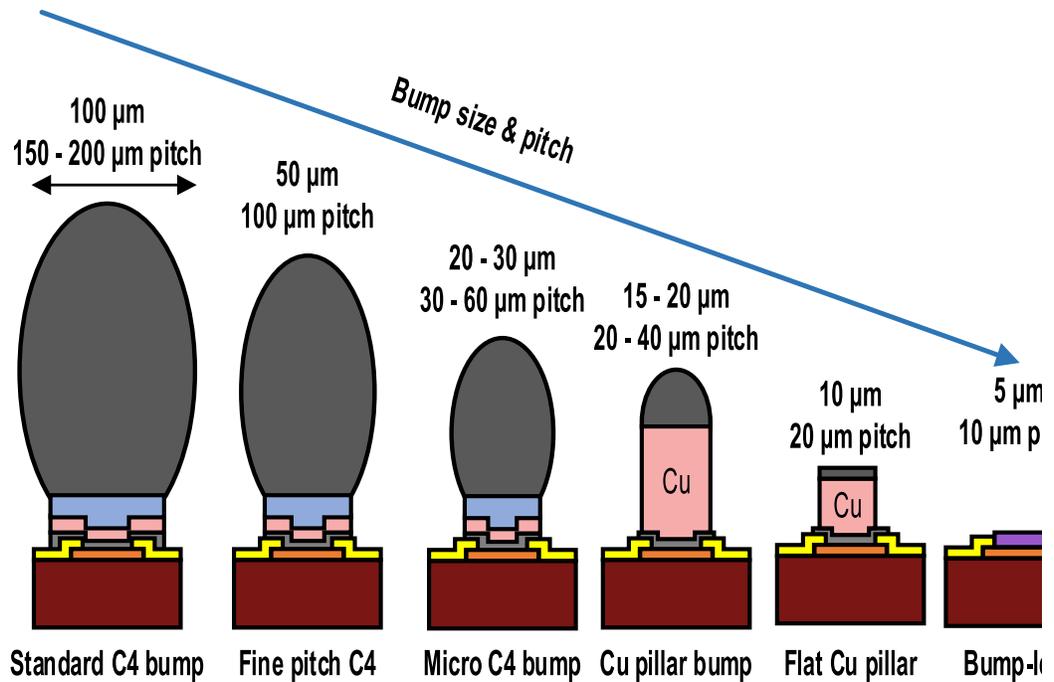


Figure 31 Trend in flip-chip bump and pitch [76]

[54]. Therefore, there is also the need to scale the CMIs to meet this trend in high-performance computing systems [55, 56].

As discussed in Chapter 2, CMIs are elastically deformable, and thus they can compensate for any surface non-uniformity on an attaching substrate. However, if a substrate has relatively large surface non-uniformity (potentially because of chip thickness differences or a die pre-attached on the substrate), CMIs could apply non-uniform reaction force along the substrate as different deformation depths induce different reaction forces, as depicted in Figure 32 (a). The non-uniform bonding force can impact the yield of bonding process bonding [57-59]. Thus, there is a need for multi-height CMIs that can apply uniform reaction force along an attaching substrate to address potential non-uniform

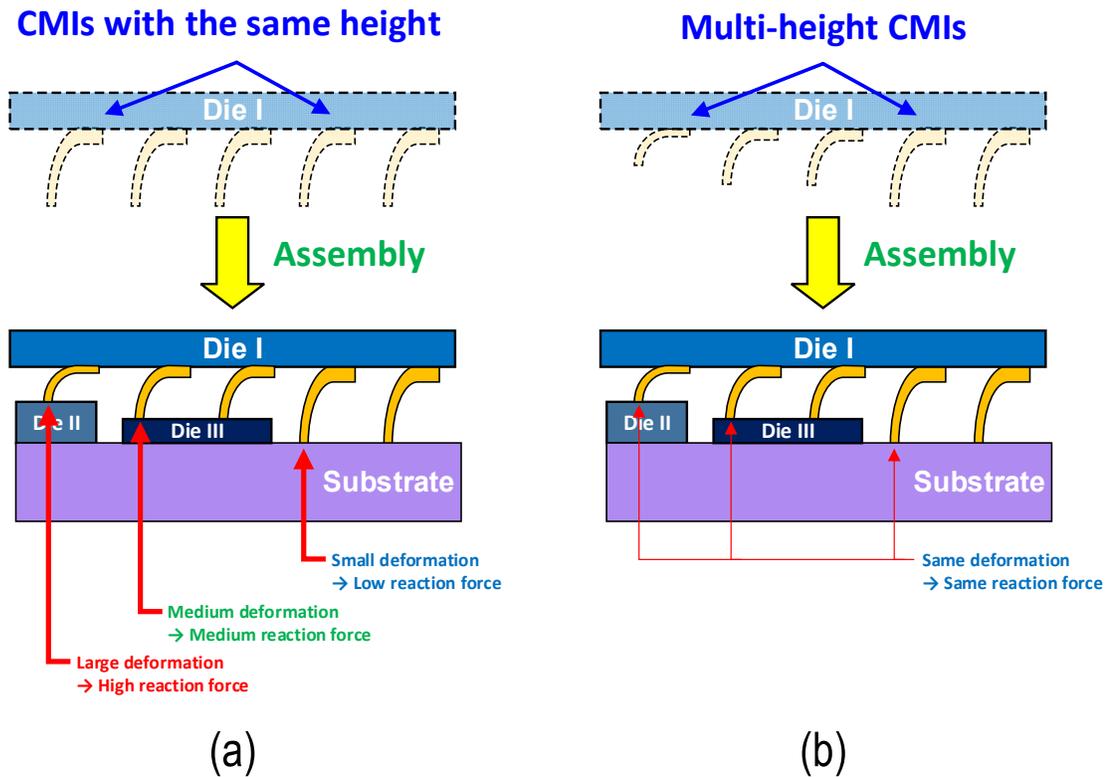


Figure 32 Assembly of CMIs with the same height (a) and multi-height CMIs (b)

bonding force issue for uniform height CMI, as shown in Figure 32 (b). The multi-height CMIs are important especially for polyolithic multi-die integration technology that we present later in this thesis.

3.1 Multi-Height CMIs

Figure 33 illustrates the fabrication process of the multi-height CMIs. The fabrication process of the multi-height CMIs is based on the fabrication process of CMIs, which was already introduced in Section 2.2. The process begins with spin coating of a sacrificial photoresist layer (AZ 40XT-11D) followed by photolithographic patterning to yield a curved sidewall profile. Next, a Ti/Cu/Ti seed layer and a second photoresist layer are deposited for electroplating. During the lithography process of the second photoresist layer, CMIs with multiple heights are easily patterned by exposing different areas on the curved sidewall profile, as shown in Figure 33 (c). After patterning the molds with various heights, NiW is electroplated within the molds to form the multi-height CMIs. Next, the photoresist layers and Ti/Cu/Ti seed layer are removed, leaving behind the free-standing

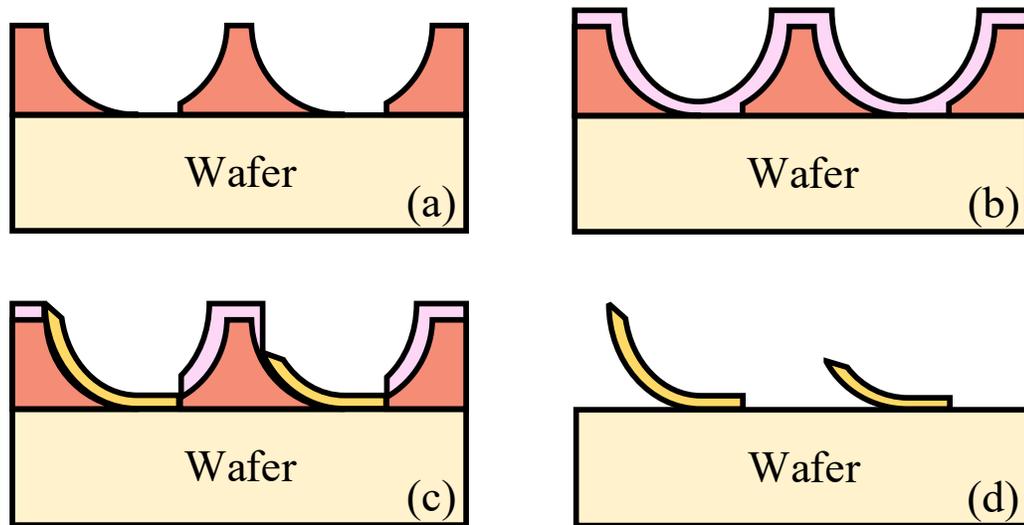


Figure 33 Fabrication process of multi-height CMIs

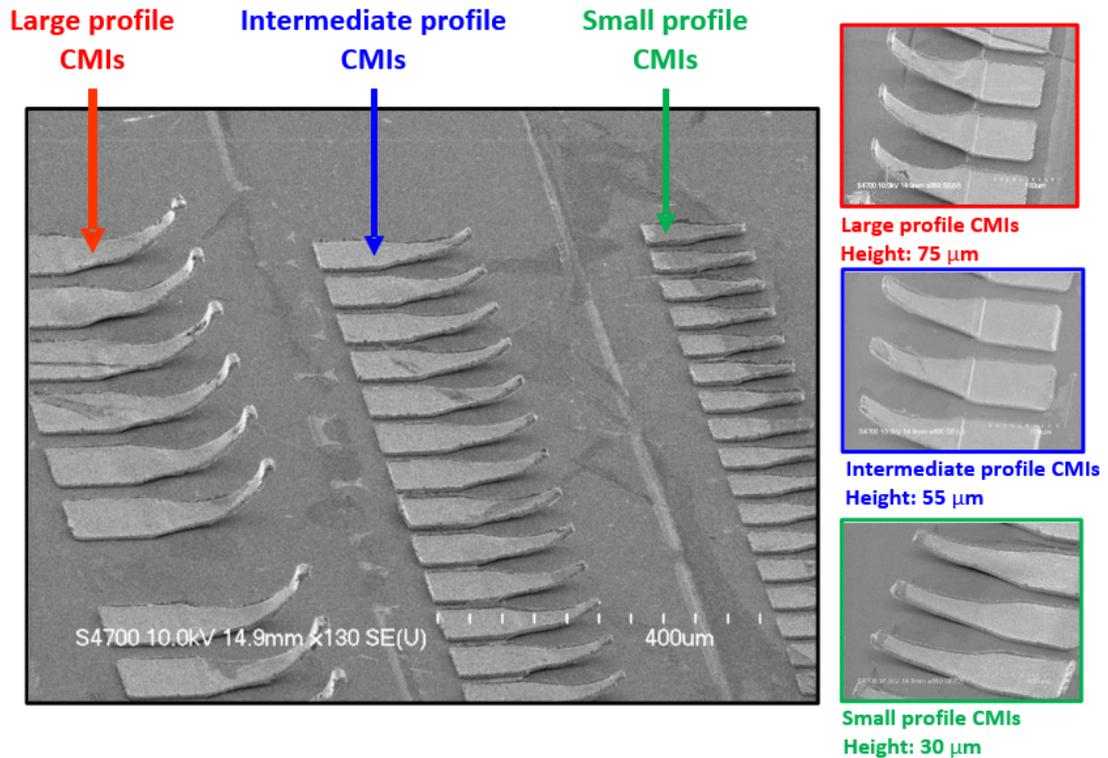


Figure 34 SEM images of the fabricated multi-height CMIs (75 μm , 55 μm , and 30 μm)

multi-height CMIs. Lastly, CMIs are passivated by electroless gold plating. Figure 34 shows SEM images of the fabricated multi-height CMIs. The heights of the fabricated CMIs are 75 μm , 55 μm , and 30 μm , and their in-line pitch is 150 μm . In order to compensate for any large surface non-uniformity, as shown in Figure 32, the height of the multi-height CMIs can be easily adjusted accordingly during fabrication.

The compliance values of the fabricated multi-height CMIs were measured using a Hysitron Triboindenter, and the results of the indentation tests are shown in Figure 35. The indentation results clearly demonstrate that the 75 μm , 55 μm , and 30 μm tall CMIs

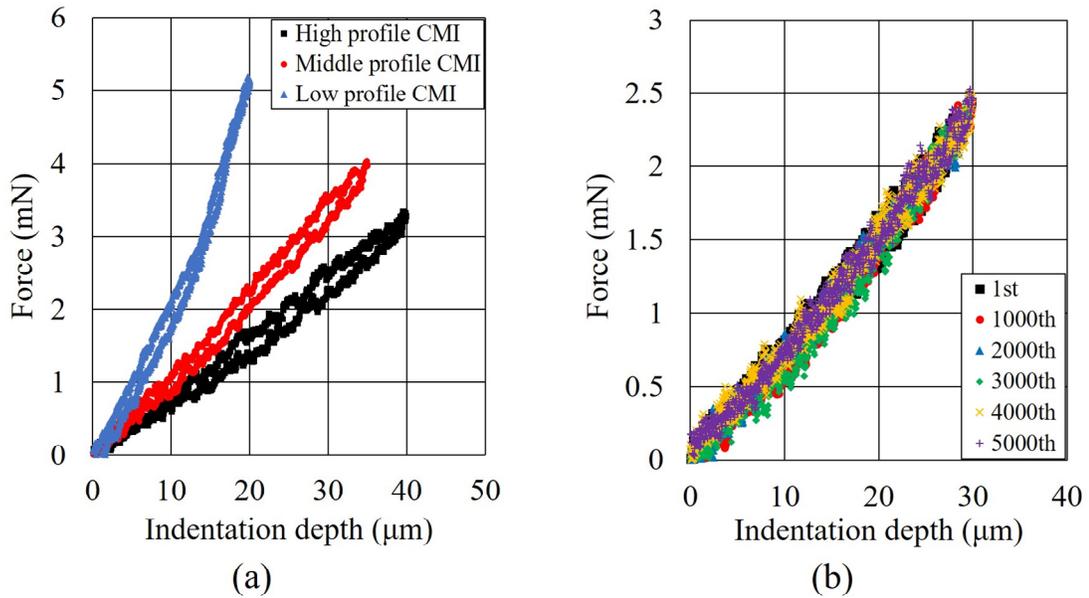


Figure 35 Force versus indentation depth curve of multi-height CMIs (a) and 5,000 cycles indentation curve of high profile CMI (b)

can achieve up to 40 μm , 35 μm , and 20 μm of vertical elastic deformation respectively, as shown in Figure 35 (a). Their respective compliances are 12.21 mm/N, 8.82 mm/N, and 3.91 mm/N. As shown in Figure 36, the compliance of multi-height CMIs decreases as the height of multi-height CMIs decreases. This change is mainly introduced by decreased CMI body length since CMI body length decreases as CMI standoff height decreases; the compliance of a typical cantilever beam is also proportional to the cube of the beam length. Note, the compliance of multi-height CMIs can be easily engineered by adjusting several parameters, such as top-view design and thickness of the CMIs, so that they can have the same compliance, as shown in Figure 32; this will be demonstrated later in this chapter CHAPTER 3. In order to test the lifetime fatigue reliability of the CMIs, one of the 75 μm tall CMIs was consecutively indented for 5,000 cycles. The tested CMI recovered its original position even after 5,000 indentation cycles, as shown in Figure 35 (b).

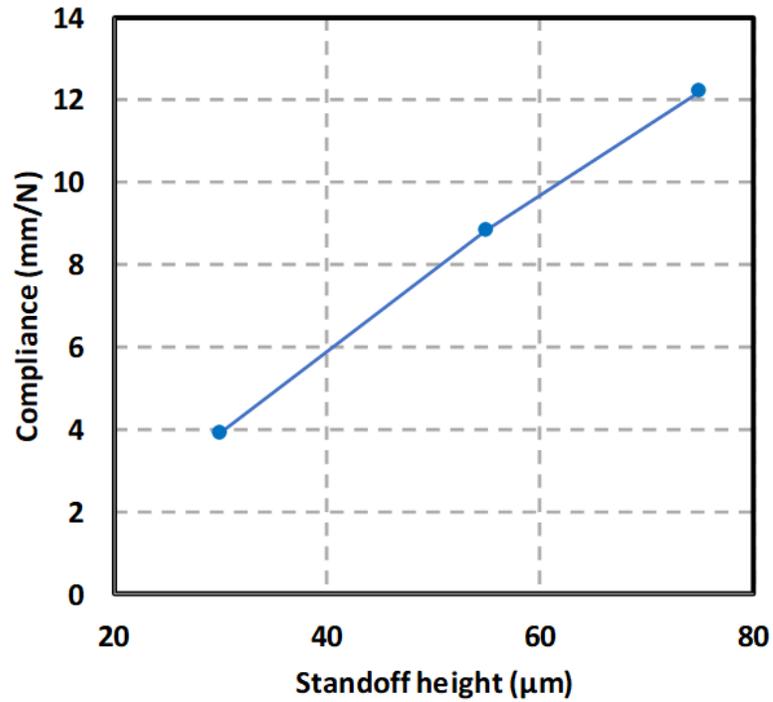


Figure 36 Compliance versus standoff height of the multi-height CMIs

Four-point probing was used to measure the resistance of the CMIs with a Karl-Suss probe station. A probe tip was directly applied to the multi-height CMIs, and the tested CMIs were partially bent to attain stable resistance readings. As shown in Figure 37, the average resistance of the 75 μm , 55 μm , and 30 μm tall CMIs was 67.17 $\text{m}\Omega$, 55.18 $\text{m}\Omega$, and 48.13 $\text{m}\Omega$, respectively.

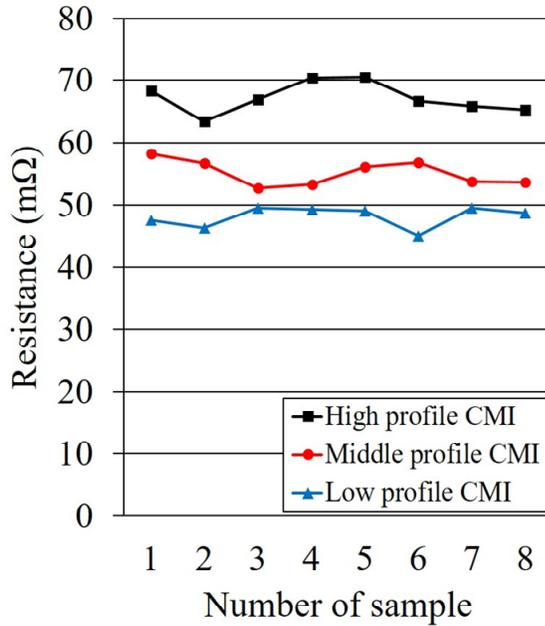


Figure 37 Four-point resistance of multi-height CMIs

3.2 Fine-Pitch CMIs

To fabricate fine-pitch CMIs, the height of CMIs needs to be scaled down along with the pitch. Thus, the fabrication of fine-pitch CMIs begins with spin coating of a thin sacrificial photoresist layer since the thickness of the sacrificial photoresist layer determines the height of CMIs. Typically, AZ 40XT-11D is spin coated to form a sacrificial photoresist layer as the photoresist is viscous. However, AZ 40XT-11D is too viscous to form a thin sacrificial photoresist layer. Therefore, AZ P4620 is used to form a thin sacrificial photoresist layer as AZ P4620 is less viscous than AZ 40XT-11D. Once a thin sacrificial photoresist layer is spin coated using AZ P4620, the rest of fabrication process is the same to that of the CMIs in Section 2.4.1. The thin sacrificial photoresist layer is

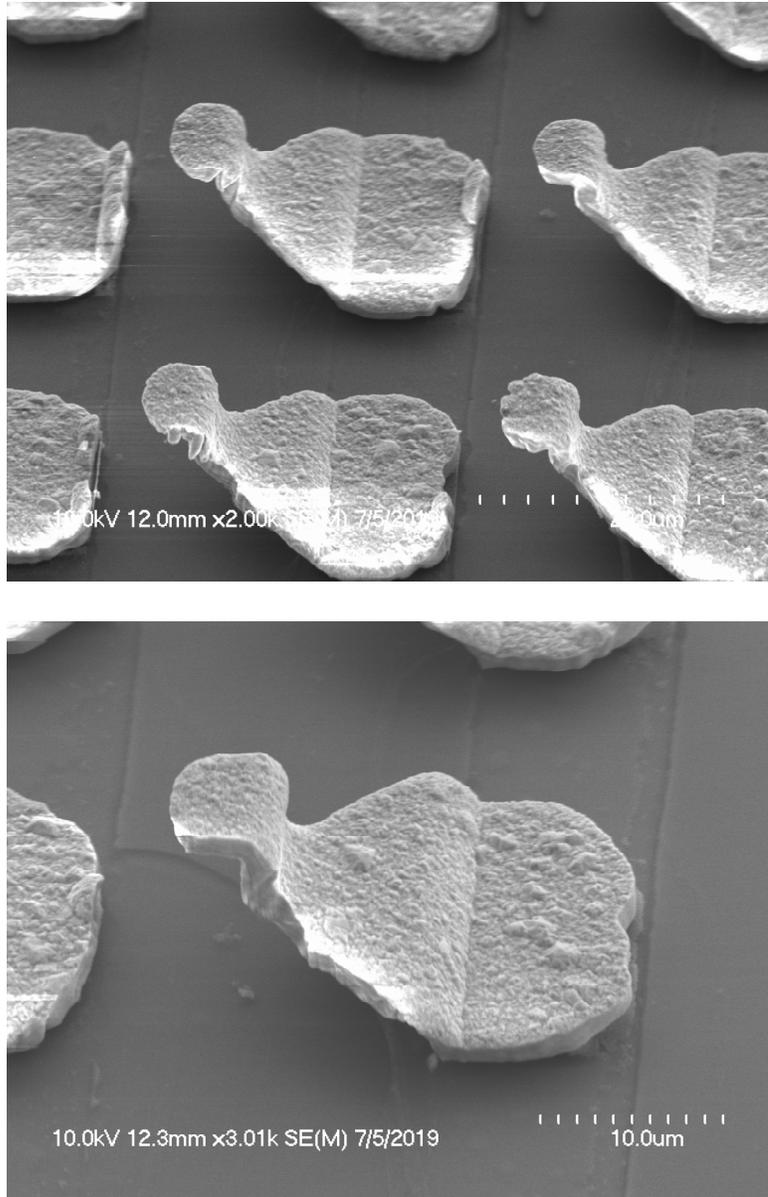


Figure 38 SEM images of the fabricated fine-pitch CMIs

patterned to form an upward curved sidewall. Next, a Ti/Cu/Ti seed layer is deposited for electroplating followed by spray coating of another photoresist to form the electroplating molds. Next, NiW is electroplated within the mold to form the CMIs. After NiW electroplating, the spray coated photoresist layer, the Ti/Cu/Ti seed layer, and the thin sacrificial photoresist layer are removed in sequence leaving behind free-standing fine-

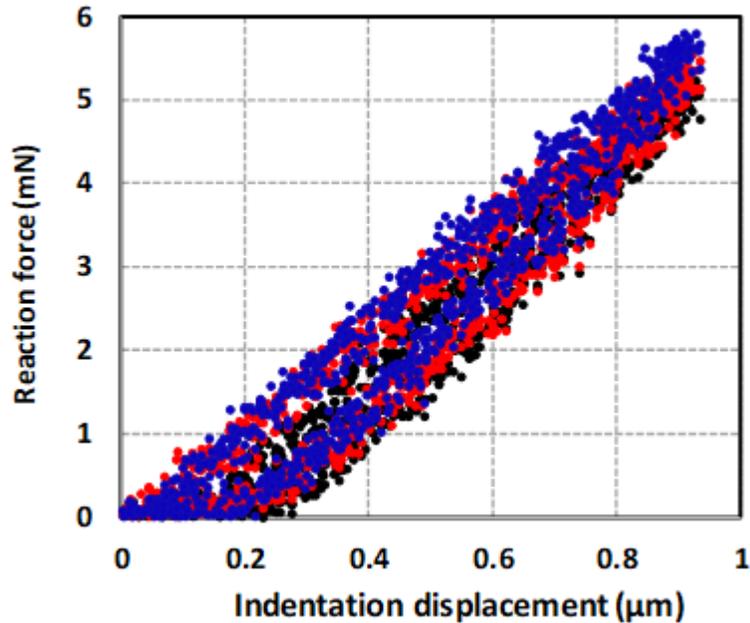


Figure 39 Compliance measurement result of fine-pitch CMIs

pitch CMIs. Finally, the fine-pitch CMIs are immersed in gold electroless plating solution to coat all exposed CMI surfaces with gold.

Figure 38 shows SEM images of the fabricated fine-pitch CMIs. The fine-pitch gold-coated NiW CMIs are approximately 9.5 μm in height, 25 μm in length, 2.5 μm in thickness, and are formed on a 30 μm x 30 μm pitch. Since CMIs are lithographically defined, they can be further miniaturized to finer pitch.

Compliance of the fabricated fine-pitch CMIs is measured using a Hysitron Triboindenter. Three fine-pitch CMIs fabricated on different regions of the chip were indented and the results of the indentation tests are shown in Figure 39. The average measured compliance of the fine-pitch CMIs is approximately 0.16 mm/N. The measured compliance is low since the thickness of the fabricated fine-pitch CMIs is 2.5 μm , which is approximately 26 % of their height (9.5 μm). In order to verify the measured compliance, the fine-pitch CMI was modeled using ANSYS FEM simulator, as shown in Figure 40. For

the simulation, Static Structural analysis system was used, and NiW material was used to form the CMI model. The ANSYS simulation parameters are summarized in Table 7. The

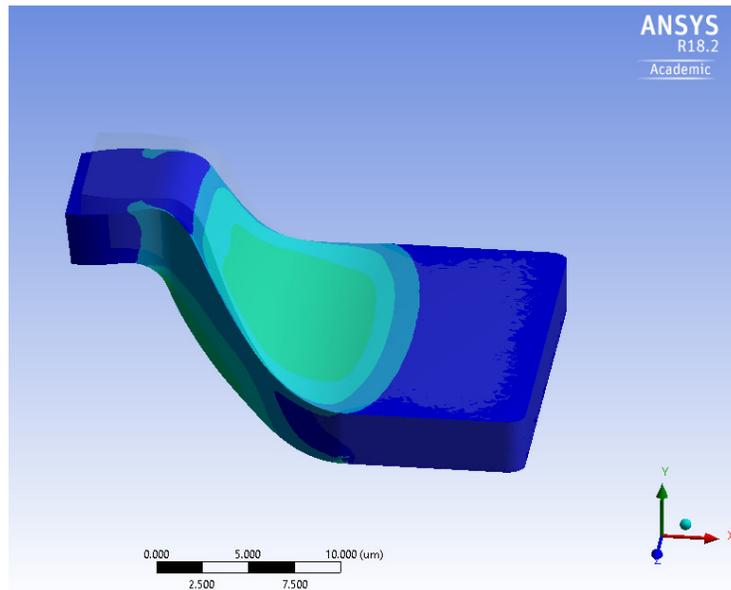


Figure 40 ANSYS FEM model of fine-pitch CMI

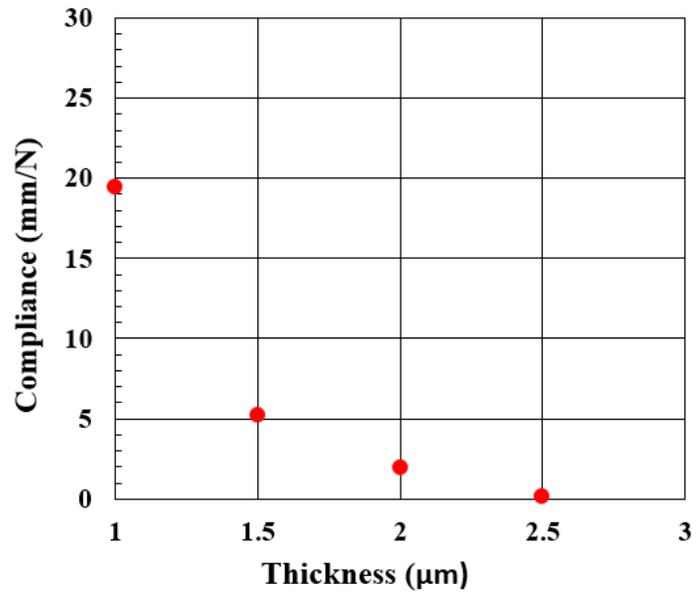


Figure 41 ANSYS compliance data as a function of thickness

Table 7 ANSYS FEM simulation setup

Analysis system	Static Structural	
Remote displacement	Y-axis: 1 μm (vertical deformation)	
CMI geometry	Height	9.5 μm
	Thickness	2.5 μm and 1 μm
	CMI body length	15 μm
	CMI anchor length	10 μm
	CMI anchor width	22 μm
CMI material	Material	NiW
	Young's modulus	1.8×10^{11} Pa
	Poisson's ratio	0.3
	Bulk modulus	1.5×10^{11} Pa
	Shear modulus	6.9231×10^{10} Pa

simulated compliance is approximately 0.169 mm/N. Additional compliance simulation data with other thickness values are shown in Figure 41; compliance increases significantly as the thickness decreases. Similar simulation results had been verified from [51], [60] as well. Therefore, this allows us to engineer a wide range of compliance values simply by adjusting the thickness of the CMIs; the thickness of CMIs can be modified by adjusting the duration of the electroplating process. Thus, a specific compliance can be attained depending on application requirements. Figure 42 shows SEM image of 1 μm thick fine-pitch CMI, and the fabrication of the very thin CMI confirms the capability of a wide range of compliance designs.

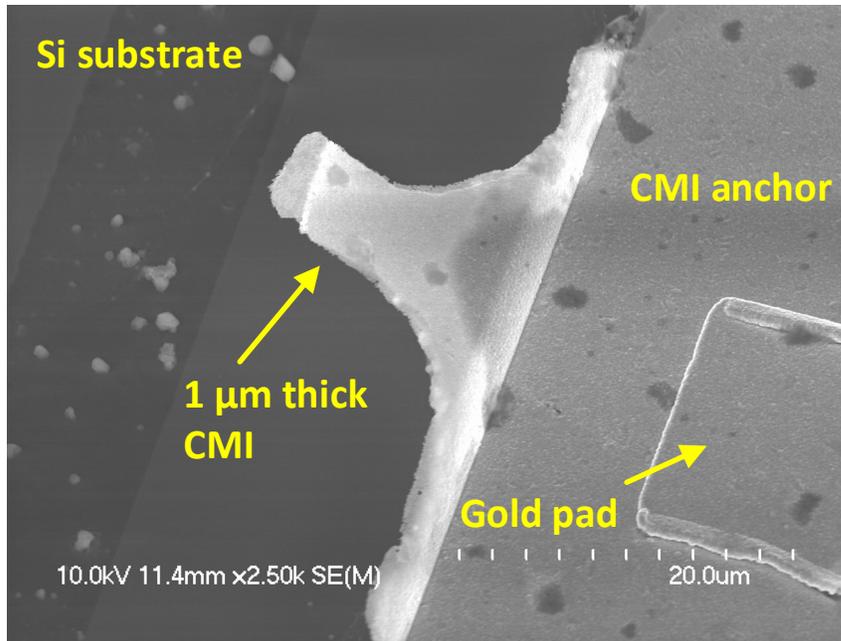


Figure 42 SEM image of 1 μm thick fine-pitch CMI

3.3 Compliance Optimization of CMIs

As noted earlier in this chapter, if a substrate has relatively large surface non-uniformity, CMIs of the same height could apply non-uniform reaction forces along the substrate as different deformation depths induce different reaction forces. Thus, there is a need for multi-height CMIs that can apply uniform reaction forces along an attaching substrate to address the potential for non-uniform bonding forces. This need can be possibly achieved by designing the compliance of multi-height CMIs to be equivalent. Several parameters, including the top-view geometric design and the thickness of the CMIs, can be used to engineer the compliance of CMIs. As demonstrated in Section 3.2, the compliance of CMIs exponentially increases as the thickness of the CMIs decreases. Therefore, we can adjust the thickness of CMIs to engineer the compliance of CMIs over a large range (i.e., coarse tuning). In addition, top-view geometric design of the CMIs can also be used to engineer the compliance of CMIs over a smaller range (i.e., fine tuning). Therefore, we need to carefully model the overall geometric design of the CMIs to match the compliance of multi-height and multi-pitch CMIs to a target compliance; this can be conducted by using ANSYS Workbench simulations. In order to demonstrate this, three types of multi-height and fine-pitch CMIs with different heights, pitches, and thicknesses

Table 8 Dimension of multi-height and fine-pitch CMIs for ANSYS simulation

Type		Height (μm)	Width (μm)	Thickness (μm)	Pitch ($\mu\text{m} \times \mu\text{m}$)
Multi-height CMIs	CMI-I	85	150	5	200 x 200
	CMI-II	35	150	5	200 x 200
Fine-pitch CMI	CMI-III	10	15	2	30 x 30

were designed and modeled using ANSYS Workbench simulator, as summarized in Table 8. Since the fabrication process of CMIs is based on photolithography, we can accommodate a large variety of geometric designs by optimizing the projected design (i.e., photomask design) of CMIs for the photolithography process. In order to optimize the projected design of the CMIs, multi-objective optimization process using a non-dominated sorting genetic algorithm-II (NSGA-II) is used [77]. We first parametrize our initial CMI design as mostly a collection of spline control points, as seen in Figure 43. These control points determine the shape of the overall spline, allowing for a very fluid exploration of

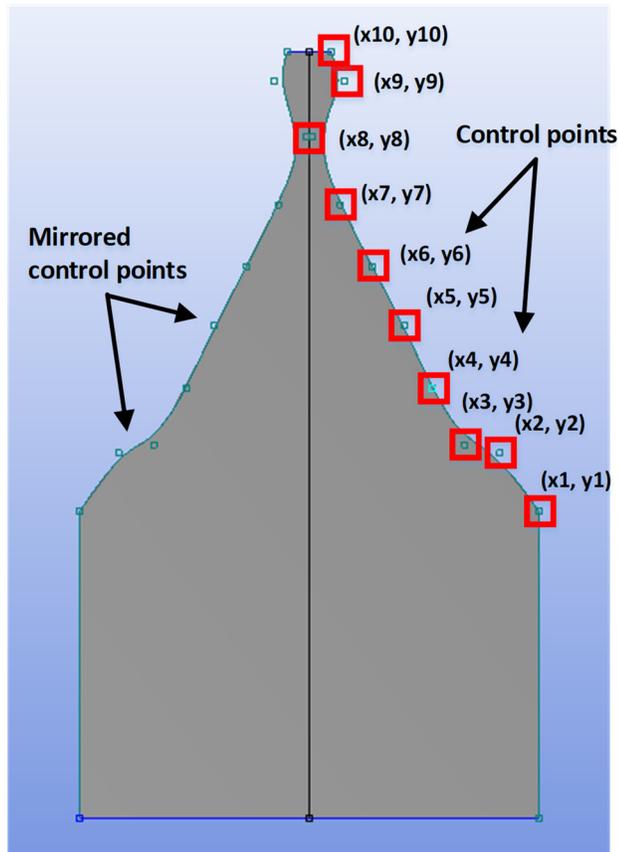


Figure 43 Parametrization of the CMI as a collection of spline control point (x, y) coordinates

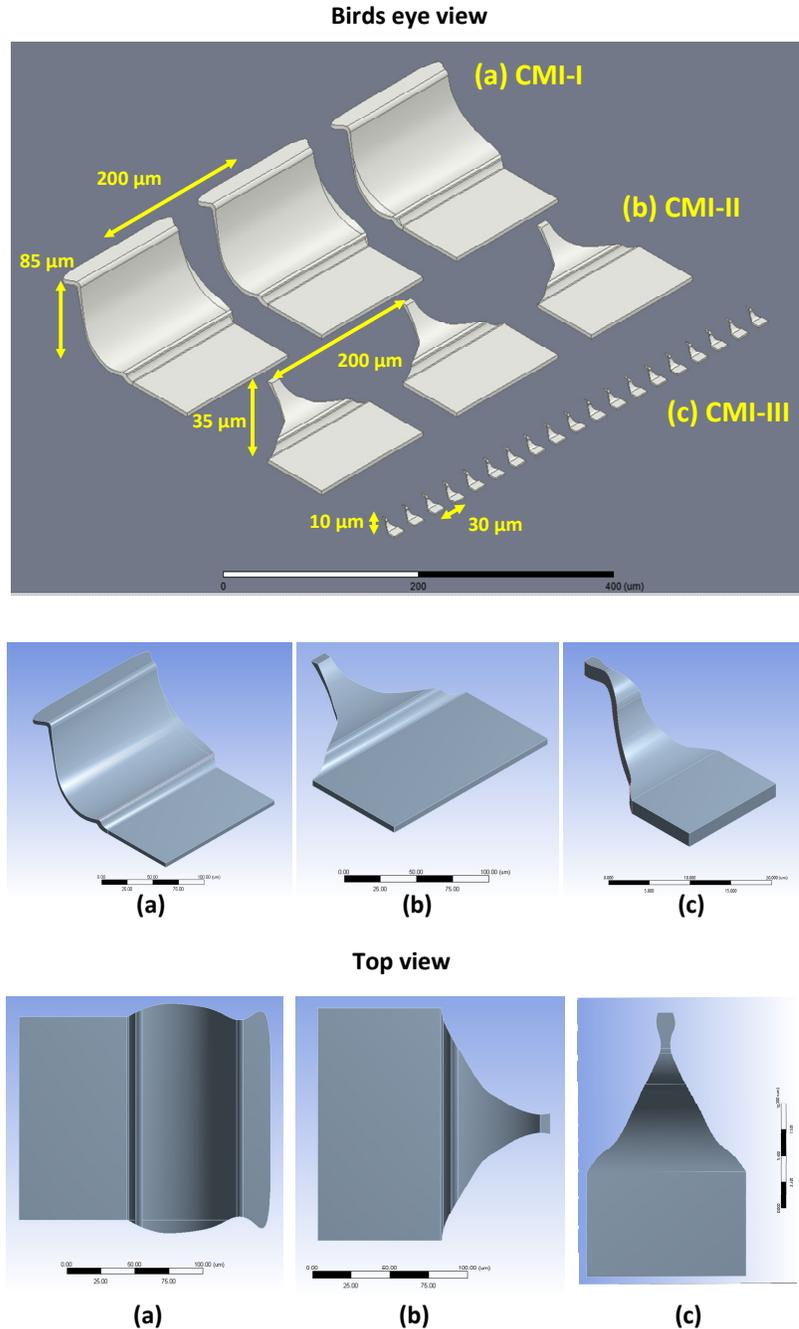


Figure 44 Optimized design of (a) CMI-I, (b) CMI-II, and (c) CMI-III

different designs. Additionally, a spline-based geometry allows for a continuity in the curvature profile of the interconnect, hence it is more likely to avoid high-stress corners relative to geometries comprised of an abrupt connection of curves, lines, etc. This

continuity in the curvature profile also helps the meshing process as stress singularities are avoided along the spline. Therefore, via modifying the (x, y) coordinates of the spline control points, the shape of the CMI mask geometry is effectively modified. After parametrizing the interconnect geometry ((x, y) coordinates), objective variables are selected for optimization. The objective variable that we seek to optimize is the mechanical compliance of the CMI. In short, our optimization process seeks to find matched compliance for multi-height and fine-pitch CMIs. Multi-objective optimization process was conducted separately for each CMI-I [H: 85 μm , P: 200 μm x 200 μm], CMI-II [H: 35 μm , P: 200 μm x 200 μm], and CMI-III [H: 10 μm , P: 30 μm x 30 μm], using ANSYS Workbench to explore designs that provide matched compliance.

Figure 44 shows the optimized designs of CMI-I, CMI-II, and CMI-III, respectively. Using ANSYS Workbench, the CMIs are indented vertically at their tips to verify the compliance, and Figure 45 and Table 9 show the indentation results. CMI-I and CMI-II are indented by 15 μm while CMI-III is indented by 1.5 μm . The simulated compliance was 1.575 mm/N, 1.504 mm/N, and 1.498mm/N, respectively for CMI-I, CMI-II, and CMI-III; this demonstrates that the compliance of multi-height and fine-pitch CMIs can be matched by optimizing the geometrical design and adjusting the thickness of the CMIs. Note that designing CMI-III to have the same thickness (5 μm) as CMI-I and CMI-II would result in approximately 0.14 mm/N compliance. Not only is this a small value of compliance, but it also becomes difficult to match its compliance to that of CMI-I and CMI-II by only changing the projected photomask design. Therefore, the thickness of CMI-III needs to be reduced from 5 μm to 2 μm in order to facilitate optimization of the geometrical design of the CMIs. If greater compliance is desired from this set of CMIs, the thickness of CMI-III

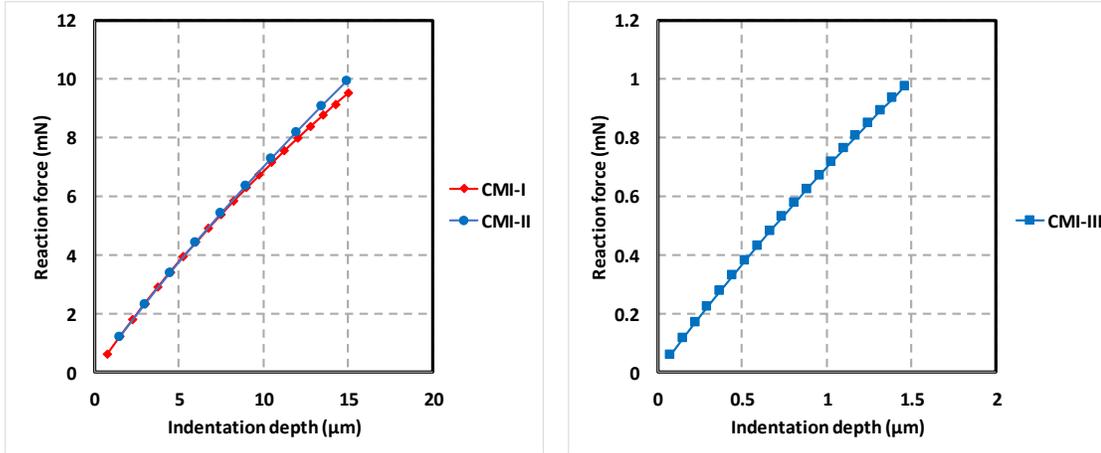


Figure 45 ANSYS indentation simulation results of the CMIs

Table 9 Simulated compliance of the CMIs

Type		Indentation depth (μm)	Compliance (mm/N)
Multi-height CMIs	CMI-I	15	1.575
	CMI-II	15	1.504
Fine-pitch CMI	CMI-III	1.5	1.498

should be reduced even further, which would result in compliance greater than 1.5 mm/N. For example, with 1 μm thick CMI-III, as fabricated in Figure 42, its compliance increases to approximately 11 mm/N.

ANSYS HFSS simulations were conducted to characterize S-parameters of the optimized multi-height and fine-pitch CMIs. We imported the ANSYS FEM model of the CMIs, as shown in Figure 44, to ANSYS HFSS, and simulated three CMIs as a G-S-G pair using a lumped port. Figure 46 shows the ANSYS HFSS model for RF simulations. In the simulated testbed, the substrate consists of 1 μm thick silicon nitride layer on a 500 μm thick silicon substrate with a resistivity of 1 $\text{k}\Omega \cdot \text{cm}$; relative dielectric constant is 7 and 11.9, respectively, within the RF range. Simulations from DC to 30 GHz are conducted by using the model, and standard nickel material is used to form the CMI body. ANSYS HFSS

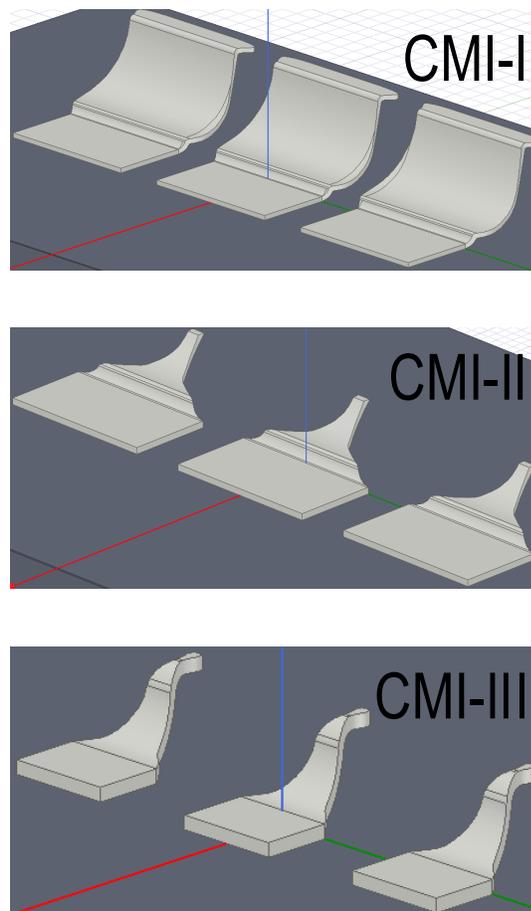


Figure 46 ANSYS HFSS model of the multi-height and fine-pitch CMIs

simulation parameters and the dimensions of the simulated CMIs are summarized in Table 10 and Table 11, respectively.

Table 10 ANSYS HFSS simulation setup

Solution type	Driven Terminal	
Port type	Lumped port	
Port impedance	50 Ω	
Frequency range	0 – 30 GHz	
CMI material	Material	Nickel
	Relative permeability	600
	Bulk conductivity	14500000 siemens/m
Dielectric layer	Material	Silicon nitride
	Relative permittivity	7
	Dielectric loss tangent	0
Substrate	Material	Silicon
	Relative permittivity	11.9
	Dielectric loss tangent	0
Radiation box	Material	Vacuum

Table 11 Dimensions of the HFSS simulated interconnects

Multi-height CMI	CMI-I	Height	85 μm
		Thickness	5 μm
		Pitch	200 μm
		CMI body length	105 μm
		CMI anchor length	80 μm
		CMI anchor width	150 μm
	CMI-II	Height	35 μm
		Thickness	5 μm
		Pitch	200 μm
		CMI body length	70 μm
		CMI anchor length	80 μm
		CMI anchor width	150 μm
Fine-pitch CMI	CMI-III	Height	10 μm
		Thickness	2 μm
		Pitch	30 μm
		CMI body length	15 μm
		CMI anchor length	10 μm
		CMI anchor width	15 μm

Figure 47 shows the simulated S_{21} and S_{11} results. As shown in Figure 47, the multi-height and fine-pitch CMIs exhibit an insertion loss of less than 0.8 dB and a return loss better than -10 dB up to 30 GHz. Because of their short length relative to wavelength, a lumped model [34] can be used to extract RLGC parasitics. The RLGC parasitics can be extracted using [34]:

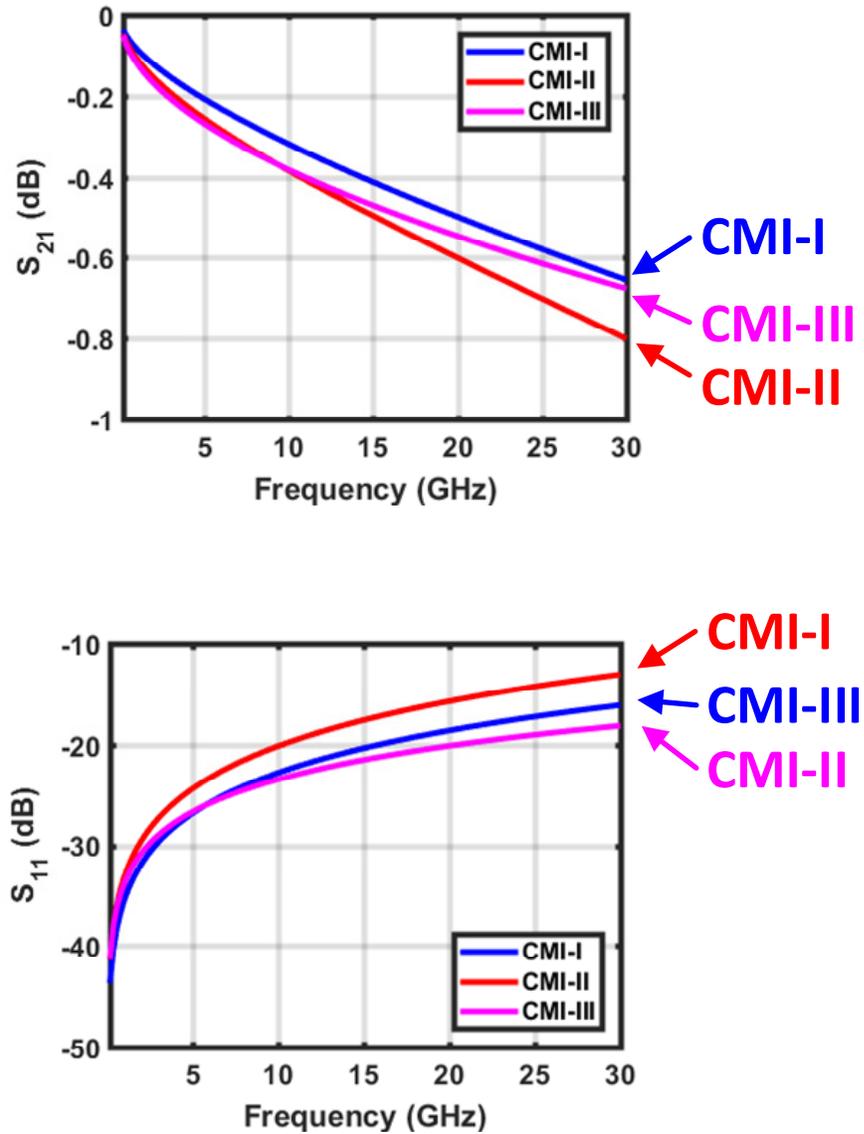


Figure 47 Simulated S-parameters of CMI-I, CMI-II, and CMI-III

$$R = \text{real}\left(\frac{-2}{Y_{12}+Y_{21}}\right) \quad (1)$$

$$L = \frac{\text{imag}\left(\frac{-2}{Y_{12}+Y_{21}}\right)}{2\pi f} \quad (2)$$

$$G = \text{real}(2Y_{11} + (Y_{12} + Y_{21})) \quad (3)$$

$$C = \frac{\text{imag}(2Y_{11}+(Y_{12}+Y_{21}))}{2\pi f} \quad (4)$$

where f is frequency.

Figure 48 shows the extracted RLGC parasitic of the simulated CMIs. Note, the dimensions of the anchors of the simulated multi-height and fine-pitch CMIs, such as width and pitch, were not designed to match characteristic impedance of 50Ω , and thus, the high-frequency

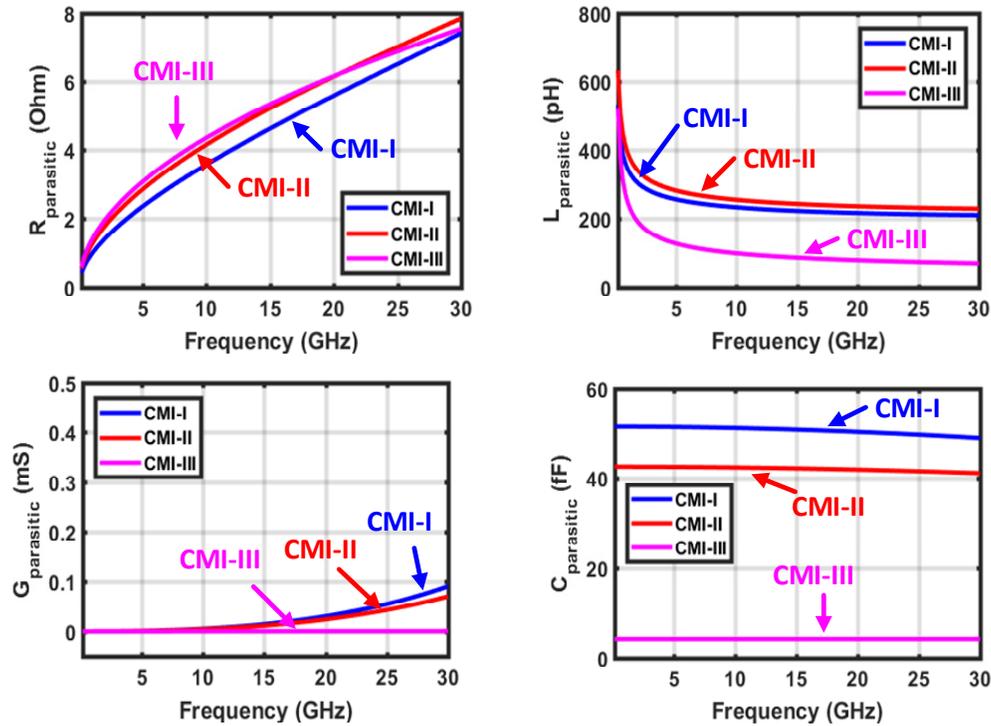


Figure 48 RLGC parasitic of the simulated CMI-I, CMI-II, and CMI-III

performance of the CMIs can be improved by matching the characteristic impedance to 50Ω . In addition to this, the high-frequency performance of CMIs can be further improved by electroless gold plating owing to skin-effect at high frequency; electric current will flow mainly through the gold surface layer instead of the NiW CMI core body due to the skin effect. Additional modeling considerations are some preliminary simulations presented later in this thesis.

3.4 Conclusion

In this chapter, the fabrication and characterization of fine-pitch CMIs and multi-height CMIs are presented. The fabricated multi-height CMIs are approximately $75 \mu\text{m}$, $55 \mu\text{m}$, and $30 \mu\text{m}$ tall, and their in-line pitch is $150 \mu\text{m}$. One of the $75 \mu\text{m}$ tall CMIs was consecutively indented for 5,000 cycles, and the CMI showed elastic motion during the indentations. The fine-pitch CMIs have $30 \mu\text{m} \times 30 \mu\text{m}$ pitch and are approximately $9.5 \mu\text{m}$ tall and $2.5 \mu\text{m}$ thick. Down to $1 \mu\text{m}$ thick fine-pitch CMI has been fabricated as well, and this confirms the capability of a wide range of compliance values. These results demonstrate a superior mechanical advantage when compared to conventional microbumps. The fine-pitch CMIs and multi-height CMIs are proposed to achieve dense signaling between ICs in addition to providing a highly scalable and versatile IC integration solution, which will be key enabling technologies for polyolithic multi-die integration technologies. This chapter also presented the design of multi-height CMIs with similar compliance based on geometry design optimization. Electrical characterization of the optimized similar compliance CMIs is also shown.

CHAPTER 4. POLYLITHIC MULTI-DIE INTEGRATION
TECHNOLOGY: HETEROGENEOUS INTERCONNECT
STITCHING TECHNOLOGY 1.0 (HIST 1.0) WITH CMIS

As discussed in Section 1.2, there is an ever increasing need to integrate multiple dice of various functionalities into a single package, and this need has spurred significant research in system-level integration technologies. While each of the technologies has benefits, they also have potential limitations, as noted in Table 12. To avoid these shortcomings, we present a Heterogeneous Interconnect Stitching Technology 1.0 (HIST

Table 12 Comparison of heterogeneous multi-die integration solutions

	HIST (this work)	Silicon Interposer	EMIB	SLIT	Chip stacking
Interconnection method	2.5-D & 3-D	2.5-D	2.5-D	2.5-D	3-D
I/O structure	Compliant interconnect & Bumps	Bumps	Bumps	Bumps	Bumps
Pitch	< 20 μm	30 – 60 μm	55 μm	45 μm	> 7.6 μm
Require TSV	No	Yes	No	No	Yes
Ability to compensate for $\Delta T/\Delta H$	Yes	Limited	Limited	Limited	-
Agnostic to package substrate	Yes	-	No	-	-
Scalability	Scalable	Limited	Scalable	Limited	Scalable (Vertical)

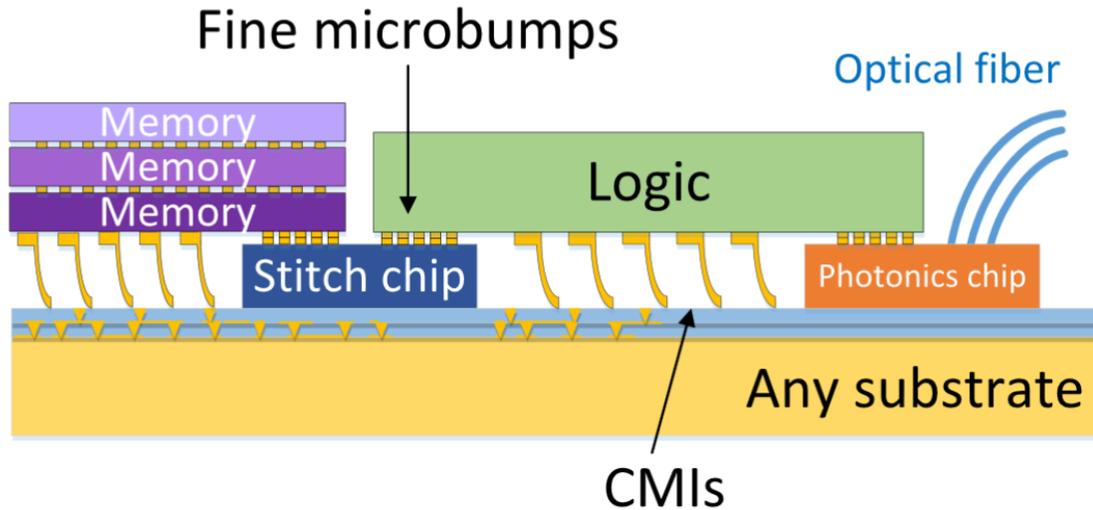


Figure 49 Schematic of HIST 1.0 platform

1.0) platform to enable the interconnection of multiple dice (or “chiplets”) of various functionalities in a manner that mimics monolithic-like performance, yet utilizes advanced off-chip interconnects and packaging to provide flexibility in IC fabrication and design, improved scalability, reduced development time, and reduced cost. Figure 49 illustrates a schematic of the HIST 1.0 platform. A stitch-chip with high-density fine pitch wires is placed between the substrate and the chiplets. In Figure 49, fine-pitch microbumps are used to bond chiplets to the stitch-chip to provide high-bandwidth density and low-energy signaling. CMIs are used to compensate for package non-planarity and enable chiplet-package interconnection. CMIs are pressure-contact based interconnects designed to mate with a pad on the package substrate. Compared to competitive solutions, the advantages of HIST platform include the following: HIST achieves a similar signal bandwidth density as the silicon interposer technology, but is not reticle-size limited, thus making it very scalable in size; HIST eliminates the need for TSVs in the substrate for decreased cost and improved signaling; HIST is based on die-to-die face-to-face bonding, and thus there are no

intermediate package levels as in the case for EMIB (i.e., package buildup layers as the embedded silicon chips are buried within the package), which enables higher signal I/O pitch and lower capacitance; and lastly, HIST can be applied to any packaging substrate (organic, ceramic, etc.) since HIST is augmented to the top-most surface of the package substrate. The presence of CMIs can also improve system mechanical reliability. In addition, the integration of silicon photonics is another promising application of HIST, as illustrated in Figure 49.

4.1 Fabrication and Assembly of HIST 1.0

In order to demonstrate the HIST 1.0 platform, a HIST testbed is design, fabricated, and measured. In this testbed, two passive chiplets emulating active dice are assembled to a stitch-chip and silicon substrate. The fabrication process of the passive chiplets begins with depositing silicon nitride on 300 μm thick silicon wafer using PECVD. Next, traces and the first layer of microbumps are patterned with Cu lift-off process followed by Au lift-off process to fabricate the second layer of microbumps. After the microbumps are fabricated, a thick sacrificial photoresist layer is spin coated onto the surface using AZ 40XT-11D. During the lithography step, a upward curved sidewall is patterned in order to form the CMI body. A Ti/Cu/Ti seed layer with thickness of 50 nm/300 nm/30 nm is deposited using sputtering followed by spray coating of a 10 μm thick photoresist layer to make electroplating molds for the CMIs. After patterning the electroplating molds, NiW is electroplated in the molds to form the CMIs. After electroplating, the spray coated photoresist layer, the Ti/Cu/Ti seed layer, and the sacrificial photoresist layer are removed in consecutive order leaving free-standing CMIs. Lastly, a thin gold layer is deposited on CMI surfaces by electroless gold plating.

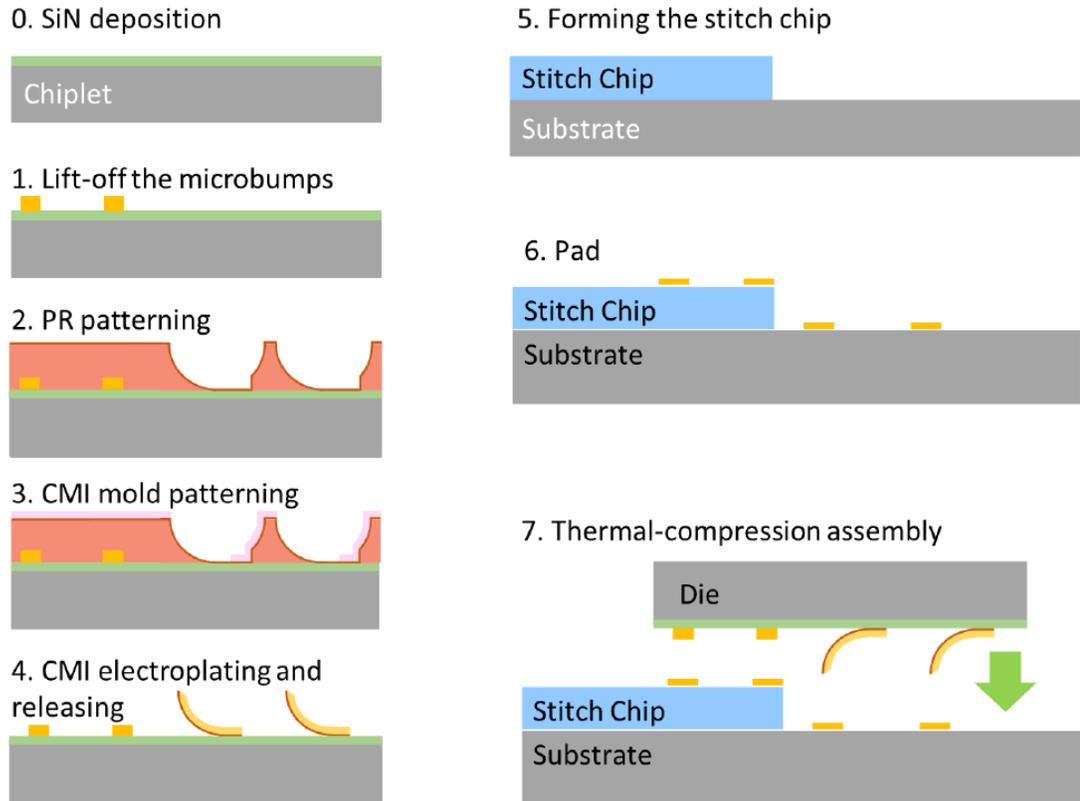
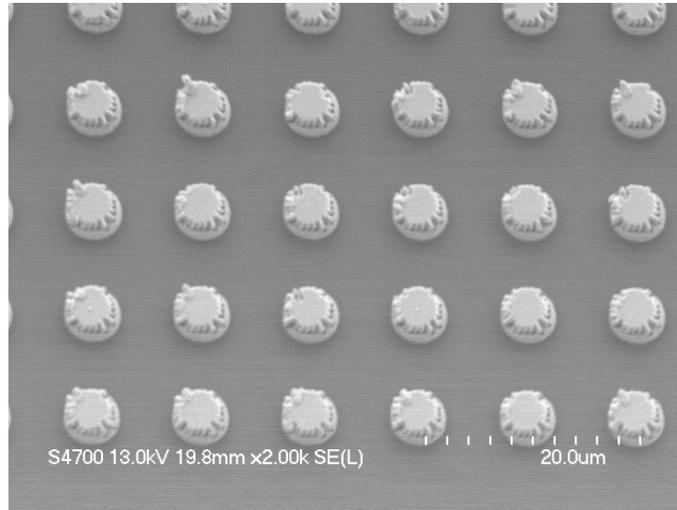


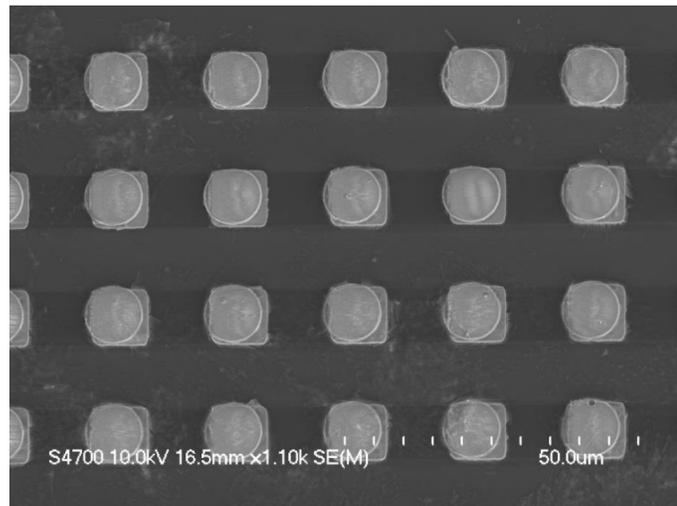
Figure 50 Overall fabrication process of the HIST 1.0 testbed

The stitch-chip is emulated by a step-like structure on the silicon substrate and formed by Bosch etching process. Next, a silicon dioxide isolation layer is deposited on the stitch-chip and the substrate followed by Cu-Au lift-off process to fabricate four-point resistance measurement structures and metal pads. Finally, the stitch-chips are singulated using a dicing saw. The overall fabrication process is shown in Figure 50.

The stitch-chip on the package substrate, which is emulated by a step-like structure, is approximately 40 μm in height. In this effort, 20 μm x 20 μm and 10 μm x 10 μm pitch Cu-Au microbumps are used to bond the chiplets to the stitch-chip. The microbumps are approximately 5 μm in height, including 3 μm of Cu and 2 μm of Au, as shown in Figure 51. The gold-coated NiW alloy CMIs are approximately 55 μm in height, 20 μm in width



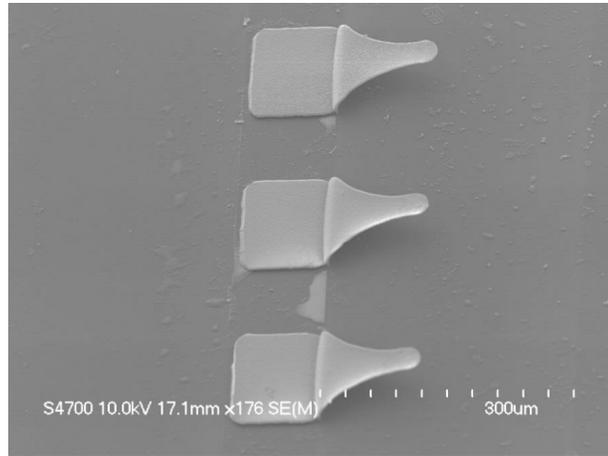
(a)



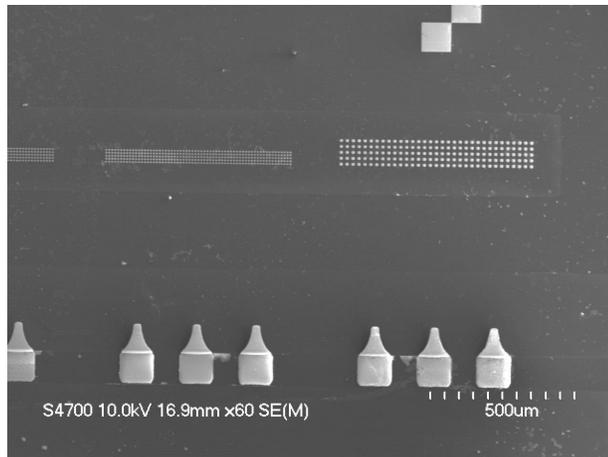
(b)

Figure 51 SEM images of the microbumps: (a) $10\ \mu\text{m} \times 10\ \mu\text{m}$ pitch and (b) $20\ \mu\text{m} \times 20\ \mu\text{m}$ pitch

at the tip, $200\ \mu\text{m}$ in length, and are on a $200\ \mu\text{m}$ in-line pitch, as shown in Figure 52. In this demonstration, both the microbumps and CMIs are fabricated on the chiplets, as shown in Figure 52 (b). In order to maximize the vertical elastic range of motion, an approximately tapered design is adopted to distribute the stress along the body of the CMI during



(a)



(b)

Figure 52 SEM images: (a) CMIs and (b) microbumps and CMIs on the chiplet

deflection. The upward-curved profile of the CMI ensures that the tip of the CMI remains in contact with the mating pad during deflection.

The fabricated two passive chiplets emulating active dice are assembled to the silicon substrate with stitch-chips emulated steps, as shown in Figure 53. The chiplets were assembled with a Finetech Fineplacer Lambda flip-chip bonder using a thermal compression bonding process. Approximately 5 N force was applied during the bonding

with maximum temperature of 300 °C. SEM and X-ray images of the assembled chiplets are shown in Figure 54. Approximately half of the chiplet is directly bonded to the stitch-

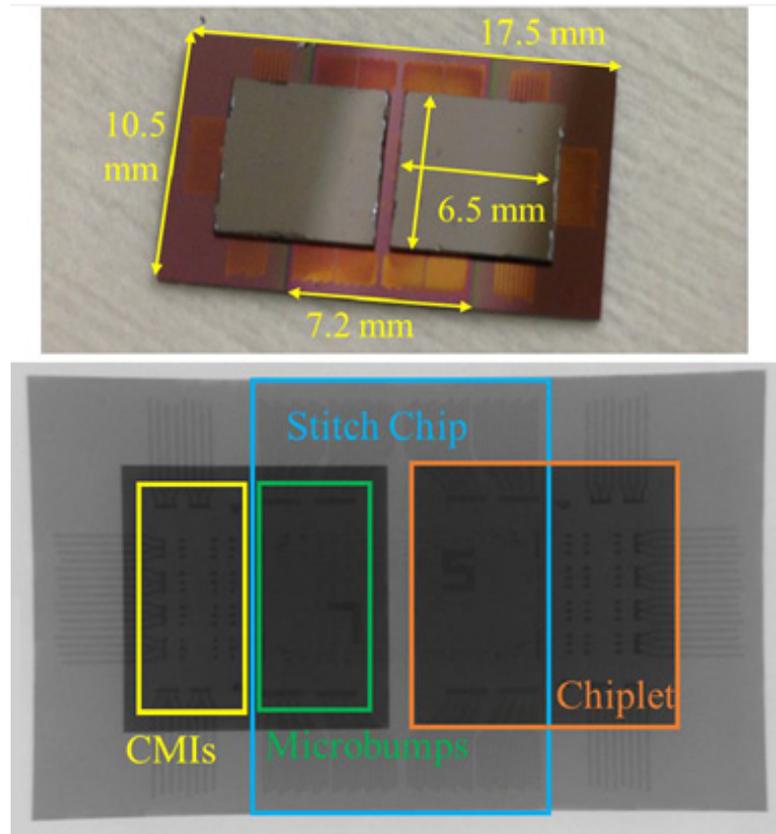


Figure 53 Micrograph and X-ray image of the HIST 1.0 testbed

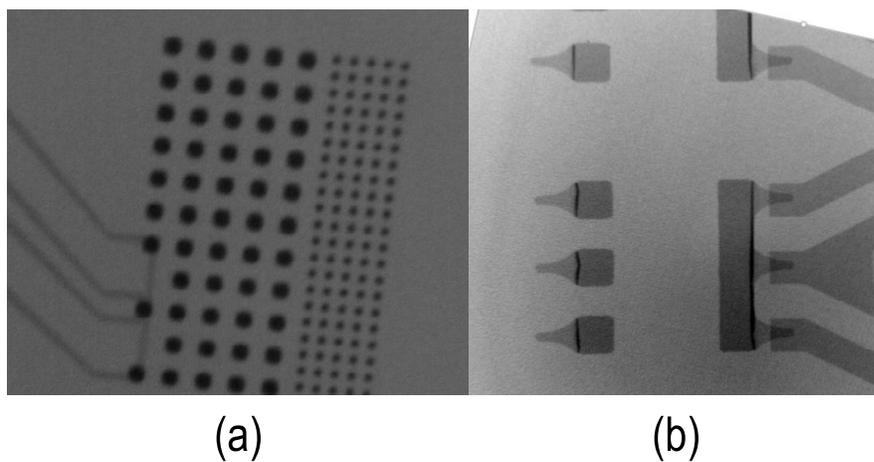


Figure 54 X-ray images of the assembled testbed: (a) microbumps and (b) CMI

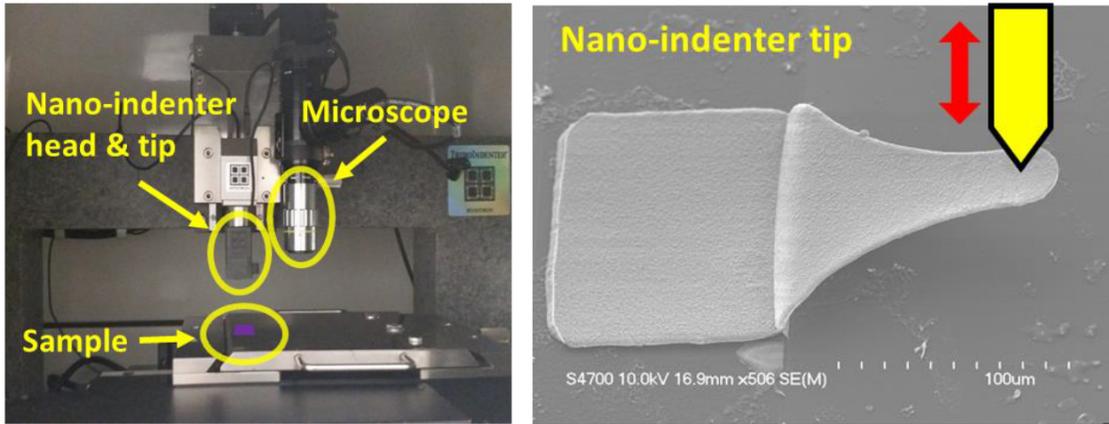


Figure 55 CMI indentation measurement setup

chip through microbumps, while the rest of the chiplet is suspended above the substrate and supported by the CMIs. Note that the CMIs, which traverse the height of the stitch-chip, are “sandwiched” between the package substrate and the chiplets to provide the needed electrical interconnection to the package substrate (power delivery and other signaling needs). For testing purposes, approximately half of the chiplet area is occupied by microbumps to support high density interconnects to the stitch-chip, while the other half is occupied by CMIs that interconnect to the package substrate. In this testbed, the dice are not underfilled. However, technologies for applying underfill within the small gap and the high-density microbumps have been demonstrated in [62] and may be used when needed.

4.2 Mechanical and Electrical Characterization

Mechanical compliance of the CMIs was measured using a Hysitron Triboindenter, as shown in Figure 55. Five CMIs located at different regions of the chiplets were measured, and the results are shown in Figure 56. The indentation results show that

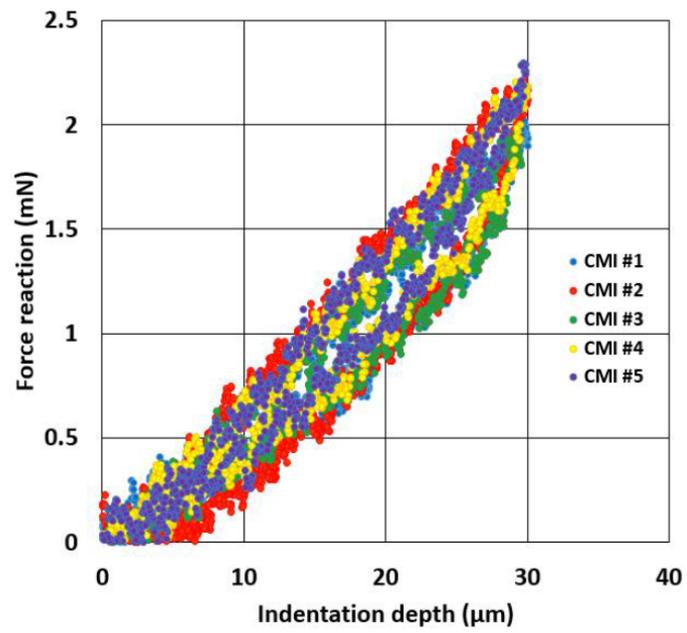


Figure 56 CMI indentation result

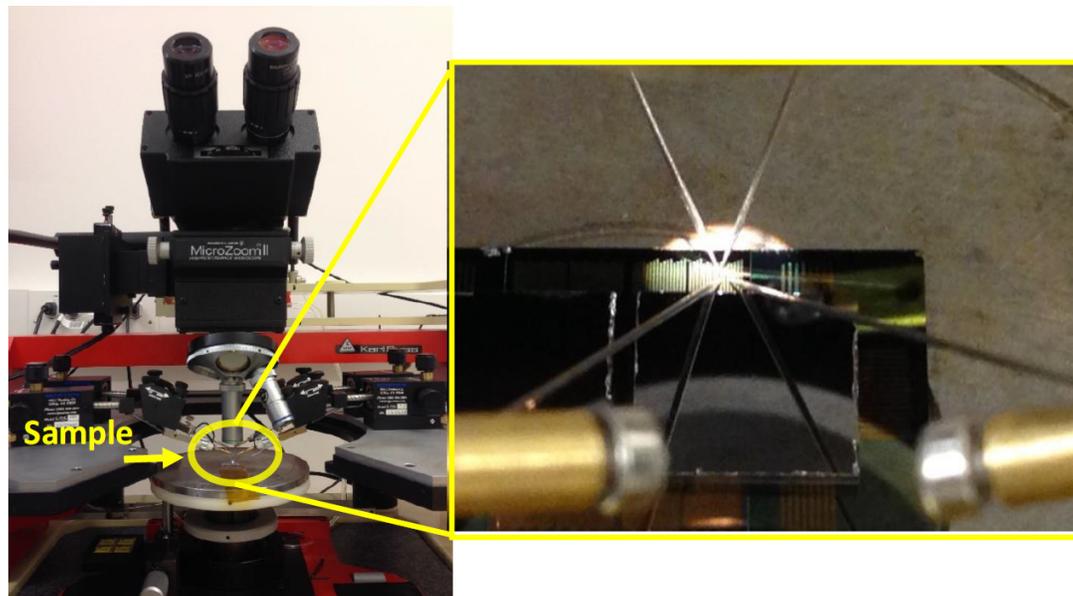
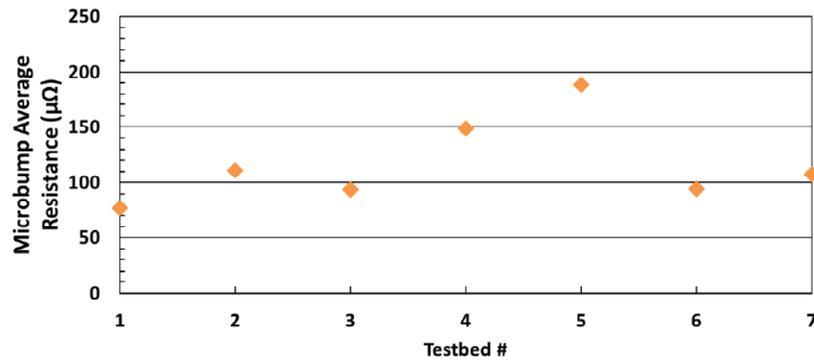


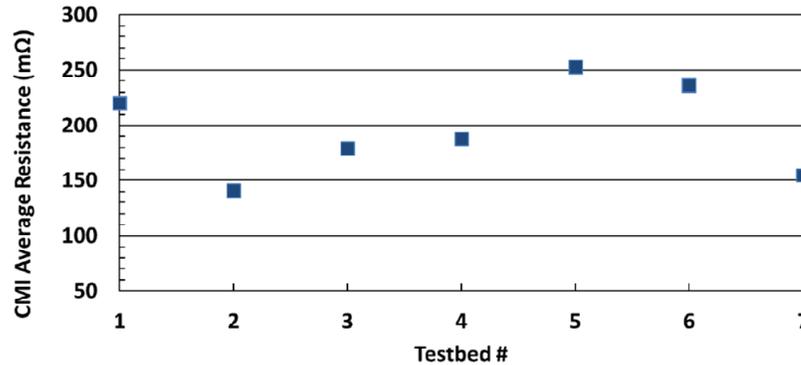
Figure 57 Four-point resistance measurement setup

the mechanical compliance is approximately 13.7 mm/N, and CMIs can achieve up to 30 μm of vertical elastic deformation.

The post-assembly resistance values of the 20 μm x 20 μm pitch microbumps and the CMIs are measured using four-point resistance structures. A Keithley 2182A voltmeter and a Keithley 6220 current source are used to perform the measurement with a Karl-Suss probe station, as shown in Figure 57. Figure 58 shows the measured four-point resistance results. The resistance of the microbumps ranges from 77.8 $\mu\Omega$ to 188.3 $\mu\Omega$. The cause of



(a)



(b)

Figure 58 Four-point resistance measurement result: (a) microbumps and (b) CMIs

the data variation is the misalignment of the assembled testbeds due to limits of our in-house flip-chip bonder. The resistance of the CMIs (including contact resistance) ranges from 141.2 m Ω to 252.9 m Ω .

4.3 Conclusion

In this chapter, a Heterogeneous Interconnect Stitching Technology (HIST) testbed is fabricated and assembled for the first time. The post-assembly electrical resistance values of the microbumps and CMIs are measured. The mechanical compliance of the CMIs is also measured. The proposed HIST platform strives to achieve monolithic-like performance, yet utilizes TSV-less high-density interconnection using stitch-chips that are integrated between the chiplets (i.e., logic-, memory-, sensors-die, etc.) and the package substrate.

CHAPTER 5. LARGE-SCALE HETEROGENEOUS INTEGRATION: HIST 2.0 WITH FINE-PITCH CMIS

We proposed a polyolithic multi-die integration technology, which we call HIST 1.0, in Chapter 4. While the first generation of HIST has many advantages for emerging heterogeneous multi-die integration, such as high bandwidth density ($10\ \mu\text{m} \times 10\ \mu\text{m}$ pitch) microbumps, we further developed the HIST 1.0 platform and proposed the next generation of the technology, which we call HIST 2.0, to enable large-scale and more flexible heterogeneous integration. Figure 59 shows the schematic of HIST 2.0. In this technology, fine-pitch (as small as $20\ \mu\text{m}$) CMIs are used to provide dense signaling pathways between the concatenated ‘anchor ICs’ through the stitch-chips instead of fine-pitch microbumps. Solder bumps, with larger pitch and height, are used for power delivery, signal routing between die and package, and mechanical interconnection between the anchor ICs and the package. The solder bumps also create the necessary force for the CMIs to form pressure-based reliable contacts. The stitch chips, which may contain high-quality passives and/or

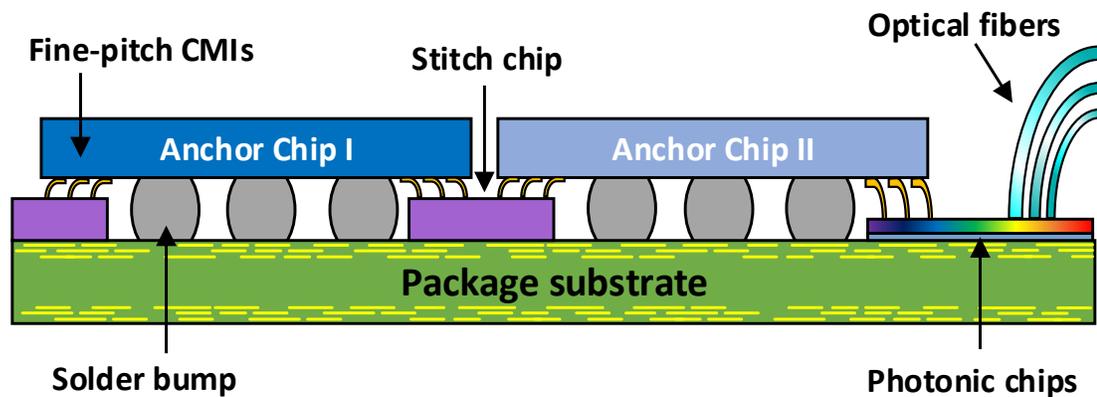


Figure 59 Schematic of HIST 2.0 enabled by fine-pitch CMIs

active circuits, in the simplest form contain only dense interconnects to interconnect nearby active anchor ICs. The anchor IC may be a logic, FPGA, MMIC, or photonic die, etc., and the surface-embedded IC may be a dense decoupling capacitor die, memory die (or stack), MEMS die, or an integrated passive device die, for example. In Figure 59, we illustrate an approach where a silicon photonic integrated circuit (PIC) with direct access to fiber assembly is face-to-face interconnected to an anchor IC using the CMIs.

The advantages of using CMIs instead of microbumps when interfacing to the stitch-chips are their ability to mechanically compensate for surface non-planarity from a stitch-chip thickness variation and interconnection gap difference between the anchor and stitch-chip as a single anchor IC can be interfaced to multiple stitch-chips on all four edges with different thicknesses. To be specific, the benefits of CMIs over conventional solder bump interconnects for multi-die heterogeneous integration are the following: a) CMIs are not susceptible to bump bridging [64], [65], which is a more prevalent issue for solder bumps as pitch is scaled down, since CMIs do not reflow during the assembly process, b) even if an anchor chip needs to interconnect with multiple stitch-chips for large-scale heterogeneous integration, CMIs can enable the interconnections with the multiple stitch-chips regardless of their thickness differences as CMIs can overcome any surface non-planarity, and c) CMIs can eliminate the need for strict controllability on chip design, which includes thickness, height, and material of substrate and height, pitch, and material of off-chip interconnects (for example, Al, Cu, and Au pads), owing to their mechanical robustness as introduced and demonstrated in Chapter 2; this can be a key benefit enabling large-scale heterogeneous integration.

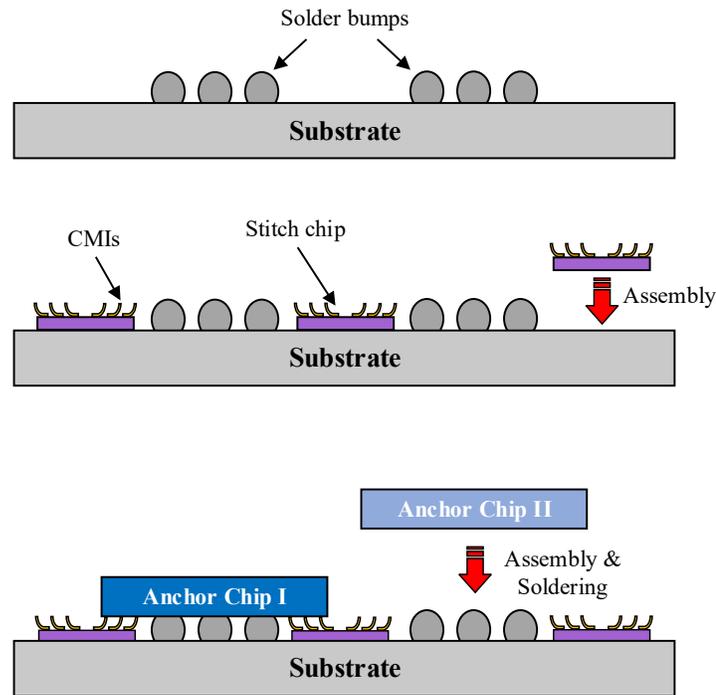


Figure 60 The integration process flow

5.1 Fabrication and Assembly of HIST 2.0

The overall integration process flow used in this work is shown in Figure 60. The Cu-Au wires are fabricated using a lift-off process and the solder bumps are electro-plated. Next, the stitch-chips with fine-pitch gold coated NiW alloy CMI's are batch fabricated and assembled on the package substrate. Finally, the anchor chips are flip-chip bonded to the package substrate. A testbed is pursued in order to demonstrate the key features of the proposed heterogeneous integration technology: assembly of chips with fine-pitch CMI's on a substrate containing stitch chips of different thicknesses and solder bumps. In this testbed, a stitch-chip on the package is emulated using a 20 μm tall step (though a larger step is possible) and the fine-pitch CMI's are fabricated on the assembled dice. The

fabricated solder bumps are approximately 50 μm in height (in general, solder bumps with larger pitch can be made taller than 100 μm [66]) and 200 μm in pitch while the lithographically-defined CMIs are approximately 40 μm in height and formed on a 20 μm in-line pitch, as shown in Figure 61 and Figure 62.

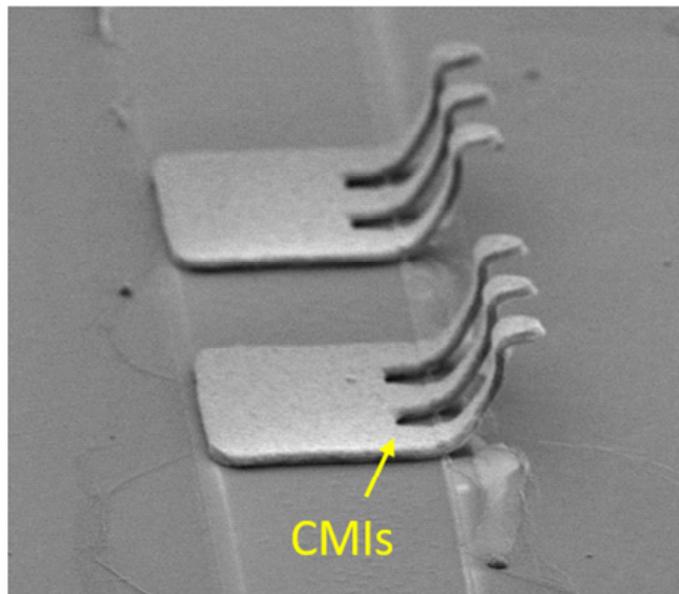
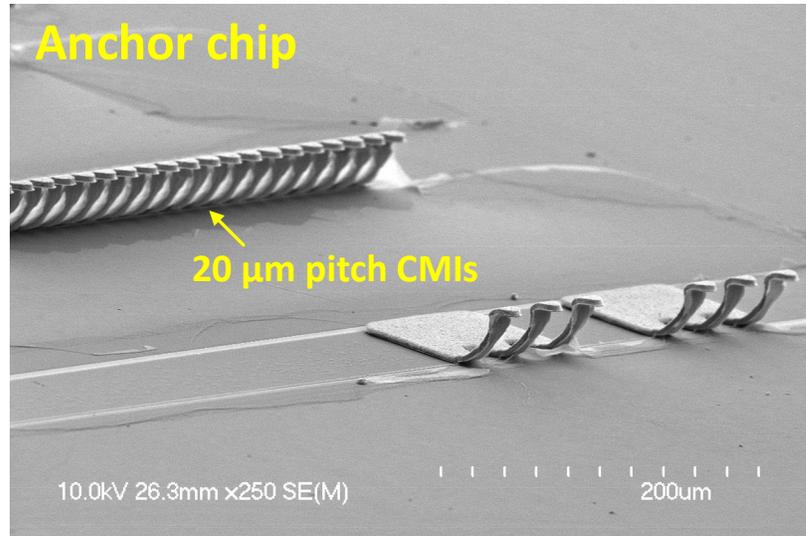


Figure 61 SEM images of the fabricated CMIs

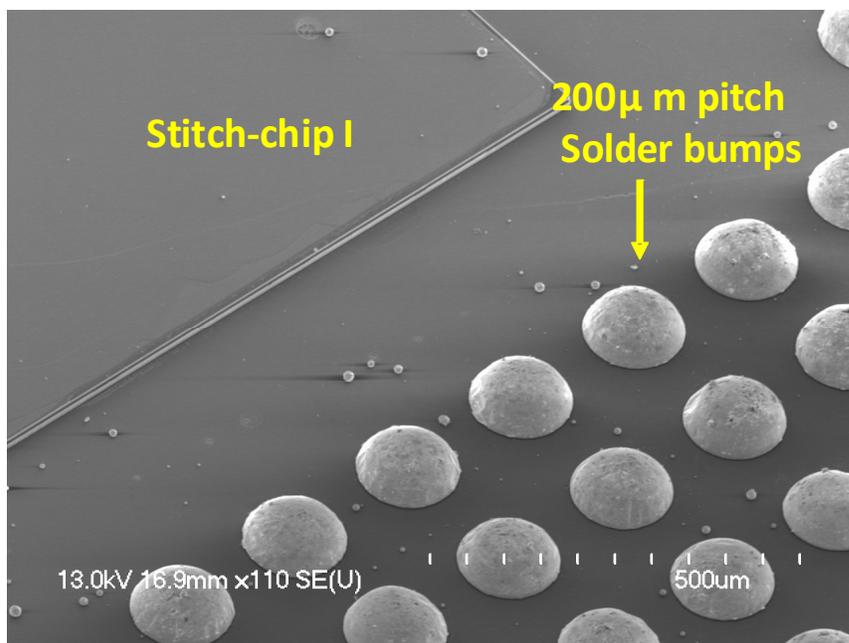
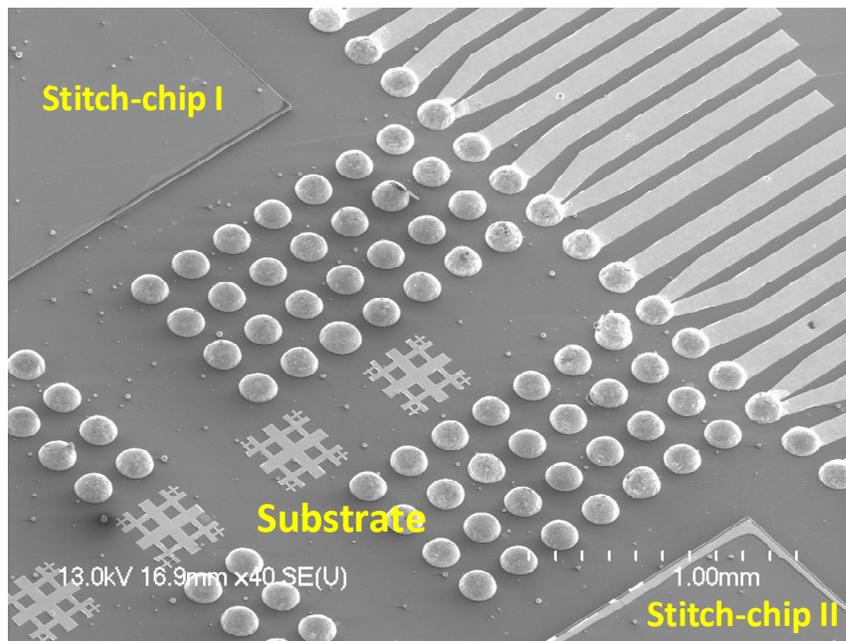


Figure 62 SEM images of the substrate with 200 μ m pitch solder bumps and stitch-chip emulated steps

Optical and SEM cross-sectional images of the assembled testbed are shown in Figure 63 and Figure 64. The dice are assembled by a thermocompression bonding process using a Finetech Fineplacer Lambda flip-chip bonder. The two anchor dice in Figure 63 are placed side-by-side onto the three stitch regions and the substrate. Once the dice are aligned to the substrate, a force is applied to compress the CMIs downward and the solder bumps are reflowed and cured to provide electrical and mechanical interconnection to the substrate; the mechanical interconnection provided by the solder bumps provides the necessary force to enable CMI reliable interconnection. As shown in Figure 64, the center

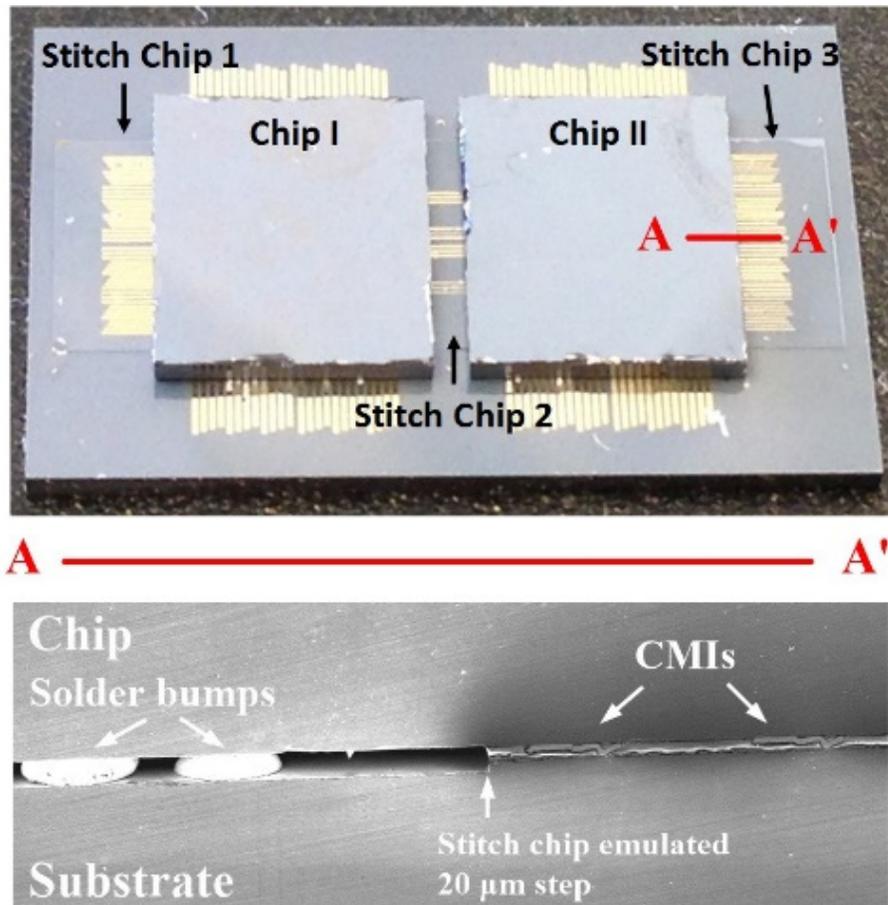
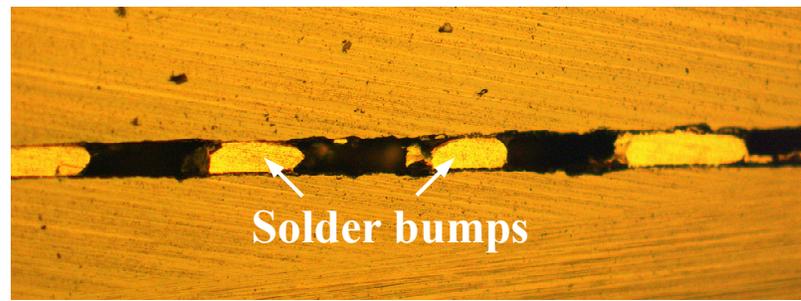
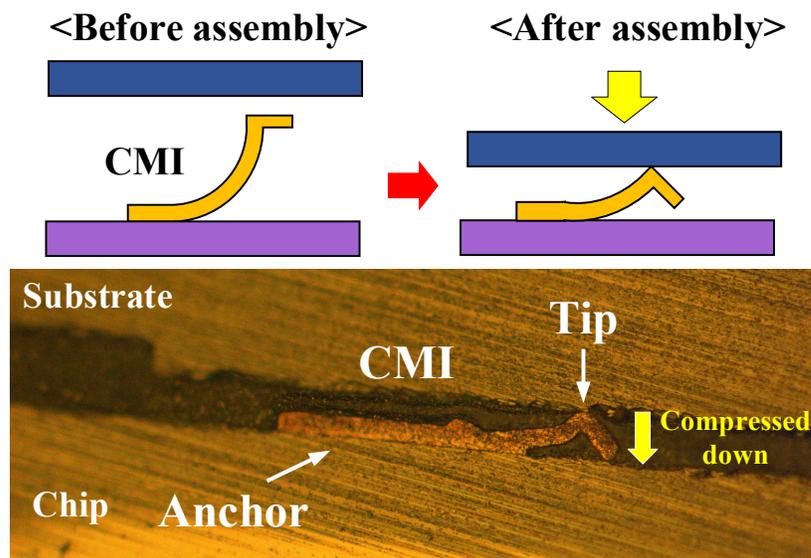


Figure 63 Optical and SEM cross-sectional image of the assembled testbed



(a)



(b)

Figure 64 Microscope cross-sectional image of solder bumps (a) and CMI (b)

of the dice is bonded to the substrate using solder bumps, while two edges of the die are suspended above the silicon steps (i.e., the ‘stitch-chips’) and supported by the fine-pitch CMIs. As shown in Figure 64 (b), the CMIs are compressed downward during assembly and form a pressure-based contact with the substrate.

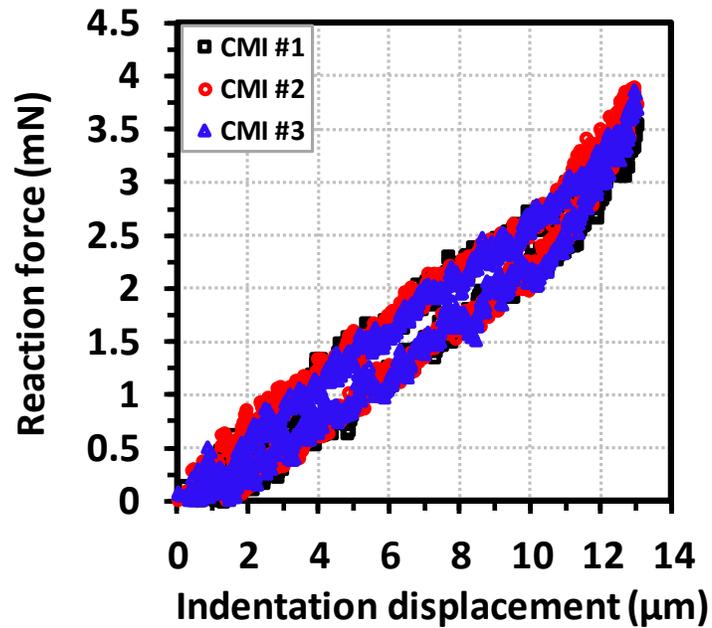


Figure 65 Compliance measurement result of the 40 μm tall CMIs

5.2 Mechanical and Electrical Characterization

Three fine-pitch CMIs fabricated on different regions of the chip were indented and the results of the indentation tests are shown in Figure 65. The average compliance of the CMIs is approximately 3.47 mm/N, and similar compliance data was obtained for the tested CMIs. As shown in Figure 65, the 40 μm tall CMIs designed under consideration achieve up to 13 μm of vertical elastic range of motion. Even if CMIs experience plastic deformation after being compressed by more than 13 μm , mechanical break does not occur, and hence they can still compensate for the stitch chip thickness variation up to their original height during assembly. Therefore, CMIs can maintain the pressure-based contact between the stitch chip and dice after assembly, as shown in Figure 64 (b). However, the mechanical attributes of the CMIs can be widely engineered due to the large design window

afforded by the fabrication process; CMI properties can vary greatly depending on their lithographically defined mold design, their thickness, their electroplated material, their height, etc. Next, chips containing fine-pitch CMIs were flip-chip bonded onto three substrates containing different stitch chip thickness mismatches ($\Delta t = 0 \mu\text{m}$, $10 \mu\text{m}$, and $20 \mu\text{m}$) and solder bumps, as shown in Figure 66. The resistances of the CMIs in contact with

Testbeds with stitch chip thickness mismatch (Δt)

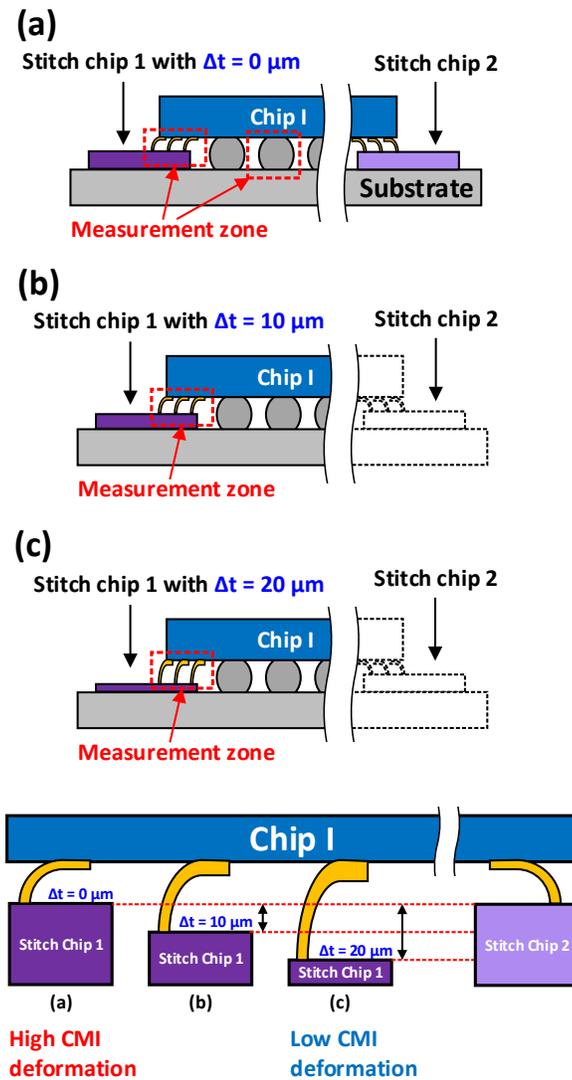


Figure 66 Testbeds with stitch-chip thickness mismatch for four-point resistance

the gold traces on the multi-height stitch chips were measured. The solder bumps were reflowed after assembly and their four-point resistance measurements were also measured. As shown in Figure 67, the average resistance of the CMIs, including their contact resistance with the gold traces on the substrate, is 146.31 mΩ, 170.02 mΩ, and 176.71 mΩ, respectively for $\Delta t = 0 \mu\text{m}$ [i.e., thicker stitch-chip], $10 \mu\text{m}$, and $20 \mu\text{m}$ [i.e., thinner stitch-chip] thickness mismatch. We assume that the contact resistance between the CMIs and the pads contributes to a difference in the average resistances seen in Figure 67 since a thicker stitch-chip deforms the CMIs more while a thinner stitch-chip deforms the CMIs less; this will affect the contact force and hence contact resistance of the CMIs. The average resistance of the solder bumps is $1.31 \text{ m}\Omega$ and we assume that variations from the

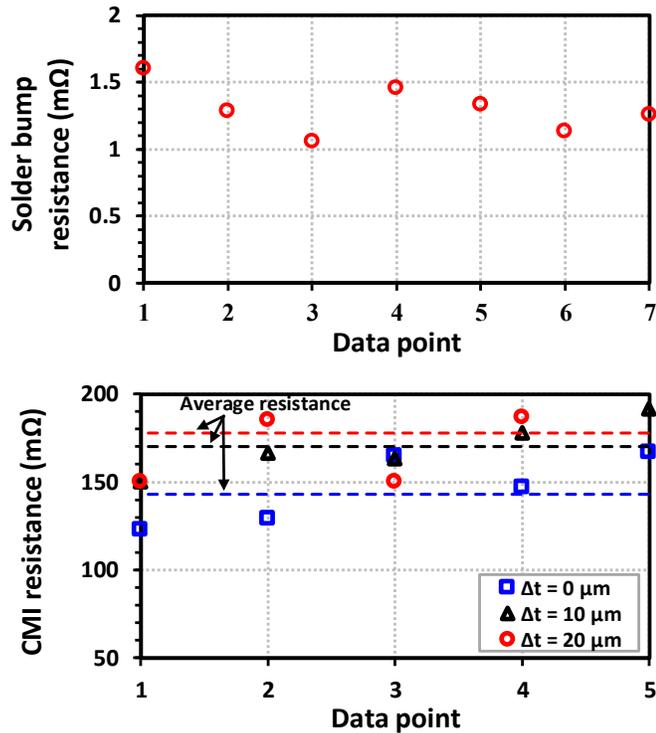


Figure 67 Four-point resistance measurement results of the solder bumps and fine-pitch CMIs

fabrication process contributed to the minor resistance variation. These four-point resistance measurement results confirm that the CMIs can maintain electrical connections between the die and the stitch-chips even when there is a stitch-chip thickness mismatch resulting perhaps from using dice of different functions from different foundries. As noted earlier, even though up to 20 μm of stitch-chip thickness mismatch has been fabricated in this demonstration, CMIs can compensate for any stitch-chip thickness variation or surface non-planarity of the substrate up to their original height owing to their mechanical flexibility.

5.3 Conclusion

This chapter presents the fabrication and assembly process of HIST 2.0 with fine-pitch CMIs. Mechanical and electrical characterizations of the assembled fine-pitch CMIs were performed, and measured results are presented to demonstrate early success. Four-point resistance measurement results for both solder bumps and fine-pitch CMIs show robust signal routing between two anchor dice through stitch-chips with low resistance variation. Fine-pitch CMIs maintain electrical connections between the die and the stitch-chips even when there is a stitch-chip thickness differences resulting perhaps from using dice of different functions from different foundries. In addition, indentation measurement results demonstrate the compliance of CMIs and their mechanical deformation. These results demonstrate the potential interconnection advantage that HIST 2.0 can provide for large-scale heterogeneous integration regardless of stitch-chip thickness variation.

CHAPTER 6. POLYLITHIC INTEGRATION OF 2.5-D AND 3-D CHIPLETS USING HIST 3.0 PLATFORM ENABLED BY MULTI- HEIGHT AND FINE-PITCH CMIS

In this chapter, in order to provide the ultimate flexibility in polyolithic integration of heterogeneous multi-die yet providing monolithic-like performance and low-loss dense signal interconnections, we propose a HIST platform that provides combined 2.5-D and 3-D integration capabilities enabled by multi-height and fine-pitch CMIs. Figure 68 illustrates a schematic of the proposed integration technology. First, the proposed integration technology provides dense 2.5-D integration by concatenating multiple anchor chips through stitch-chips, which are placed between the anchor chips and the package substrate. Fine-pitch CMIs on the edges of the anchor chips provide high bandwidth interconnection between the anchor chips through the stitch-chips [67]. ‘Surface-embedded chips,’ which may be passive or active dice, are integrated underneath the anchor chips and are interconnected using face-to-face 3-D bonding using CMIs. Multi-height CMIs are utilized to enable the face-to-face direct interconnections between the anchor chips and the surface-embedded chips. This approach can also enable direct interconnection between an anchor chip and a silicon photonic integrated circuit (PIC) with direct fiber assembly, as illustrated in Figure 68. Power delivery and signal interconnections from the package substrate can also be enabled by the multi-height CMIs. Mechanical bonding between the anchor chips and the package substrate is enabled by using large solder bumps on each of

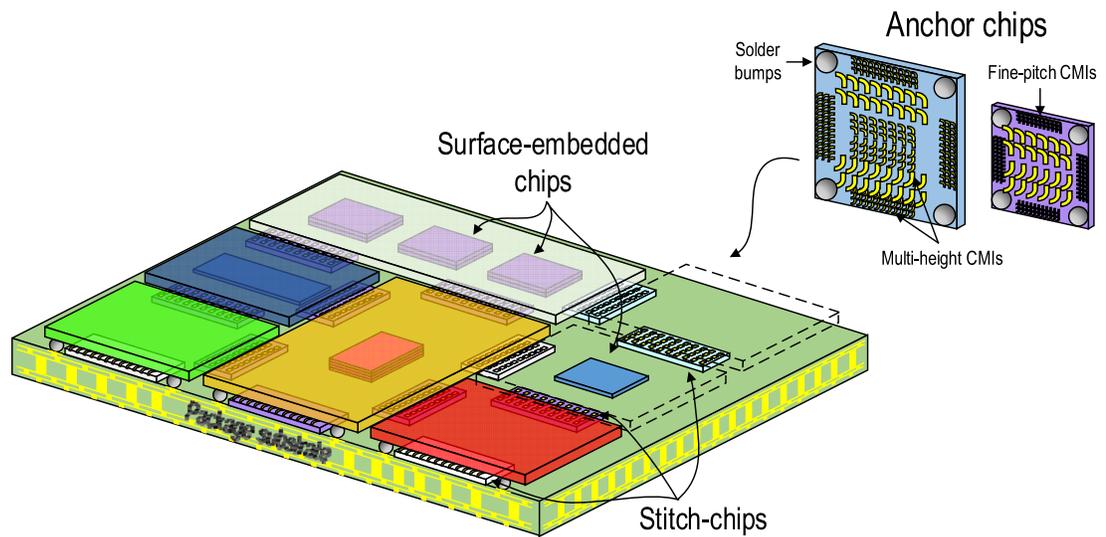
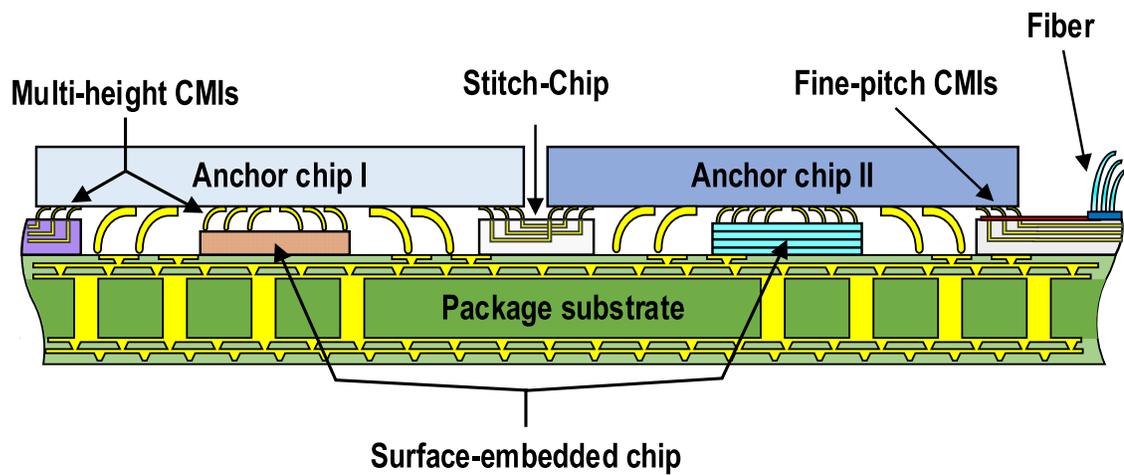


Figure 68 Schematic of polyolithic integration for heterogeneous dice using multi-height and fine-pitch CMI

the four die corners to enable reworkability of the assembled die. Since the CMI are elastically compressible unlike conventional solder bumps, the proposed polyolithic integration technology can compensate for any possible off-chip interconnection distance

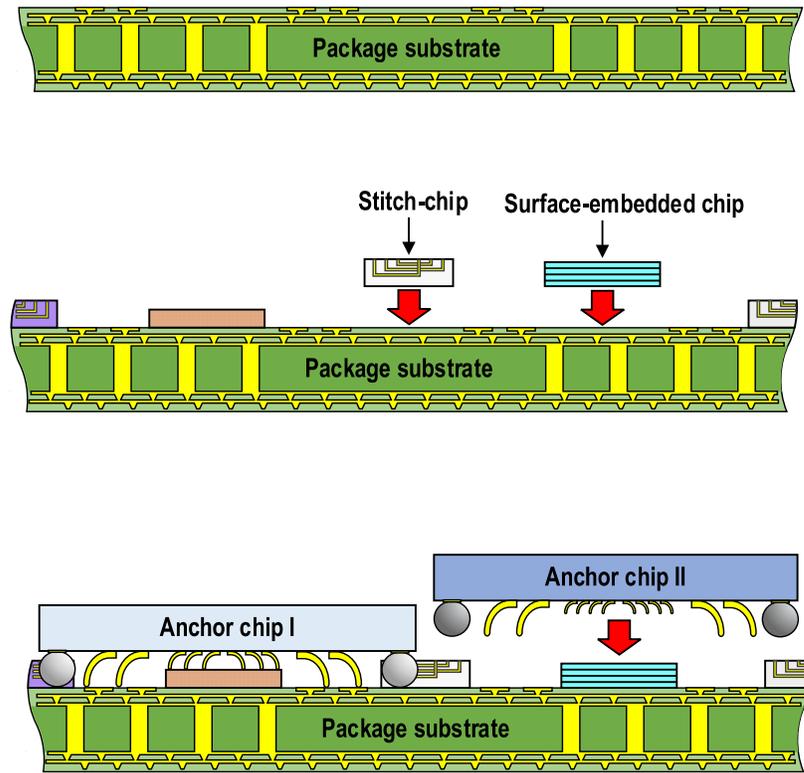


Figure 69 The assembly process flow

differences resulting from chip thickness differences; this enables both 2.5-D and 3-D face-to-face interconnection in one platform, as shown in Figure 68. In addition, CMIs can provide temporary interconnection, which can improve package and system yield as CMIs facilitate die replacement/rework. The mechanical compliance of the CMIs can also improve the thermomechanical reliability of the assembled system [68] as well as enabling flexibility in dice and substrates to be stitched together irrespective of CTE mismatch (e.g., silicon, glass, organic, and GaN).

6.1 Fabrication and Assembly of Stitch-Chip Based Polyolithic Integration

Figure 69 shows the overall assembly process flow of the proposed HIST 3.0. The integration process begins with forming traces and pads on the package substrate. Next, the stitch-chips and/or surface-embedded chips are attached onto the package substrate. The anchor chips with multi-height CMIs and relatively large solder bumps are flip-chip bonded onto the package substrate, as shown in Figure 69 (note, CMIs can be on the stitch-chips instead). Finally, the assembly is completed by reflowing the solder bumps. As discussed in Chapter 2, NiW is used again to form the core of the CMIs due to its high yield strength of 1.93 GPa. The NiW CMIs are electroless gold plated as the final fabrication step to prevent oxidation.

The testbed is fabricated and assembled in order to demonstrate the key features of the proposed technology: assembly of an anchor chip with multi-height CMIs onto a

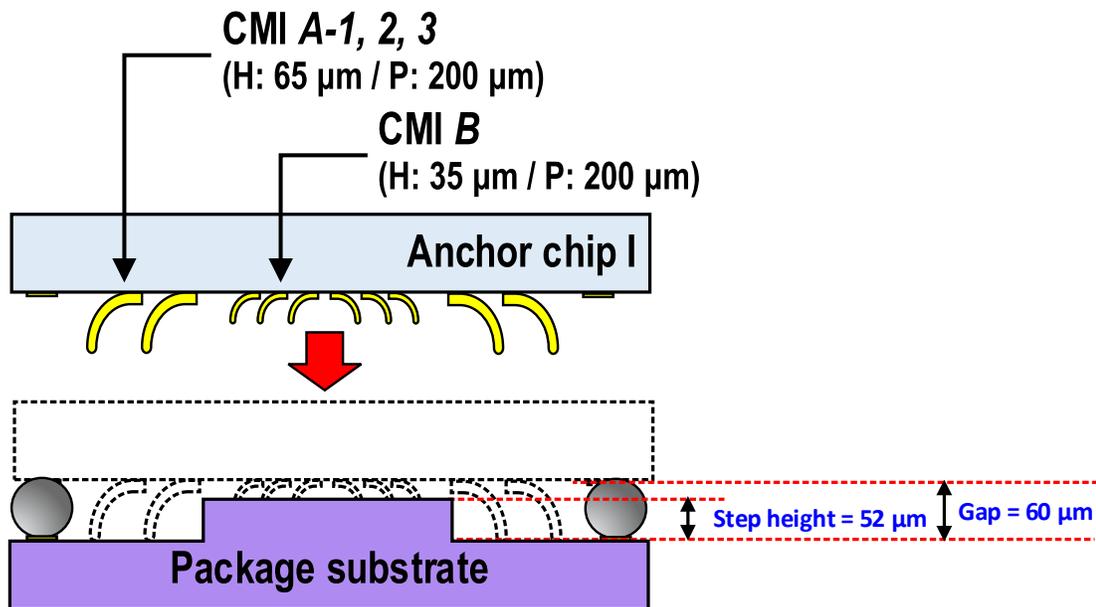


Figure 70 Schematic of the fabricated testbed

substrate with a surface-embedded chip and mechanical bonding using solder bumps. In the testbed, the surface-embedded chip on the package substrate is emulated by forming a tall step on the silicon substrate. Four solder bumps are also fabricated on the silicon substrate to mechanically secure the assembled testbed. For the anchor chip with multi-height CMIs, two CMI designs with different heights, which we refer to as CMI A and CMI B in this chapter, are fabricated on a silicon substrate. Both fabricated CMI A and B have $200\ \mu\text{m} \times 200\ \mu\text{m}$ pitch while the heights are approximately $65\ \mu\text{m}$ and $35\ \mu\text{m}$, respectively. Specifically, for CMI A, three different CMI designs (A-1, A-2, and A-3) of the same height are designed to demonstrate the simplicity of CMI compliance engineering. Figure 70 shows a schematic of the fabricated testbed. Note, in Chapter 2, we demonstrated the fabrication of CMIs with $20\ \mu\text{m}$ of in-line pitch and $30\ \mu\text{m} \times 30\ \mu\text{m}$ pitch.

SEM images of the fabricated anchor chip are shown in Figure 71 and Figure 72. An approximately tapered design is used for the different CMI designs in order to distribute the stress along their length during deformation. The upward-curved cross-sectional design ensures that the tip of the CMI maintains contact with the corresponding pad during assembly.

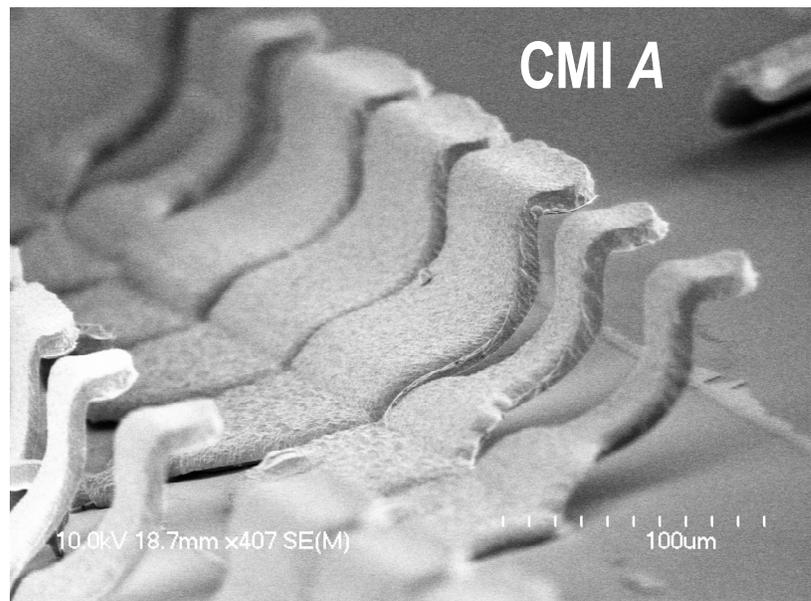
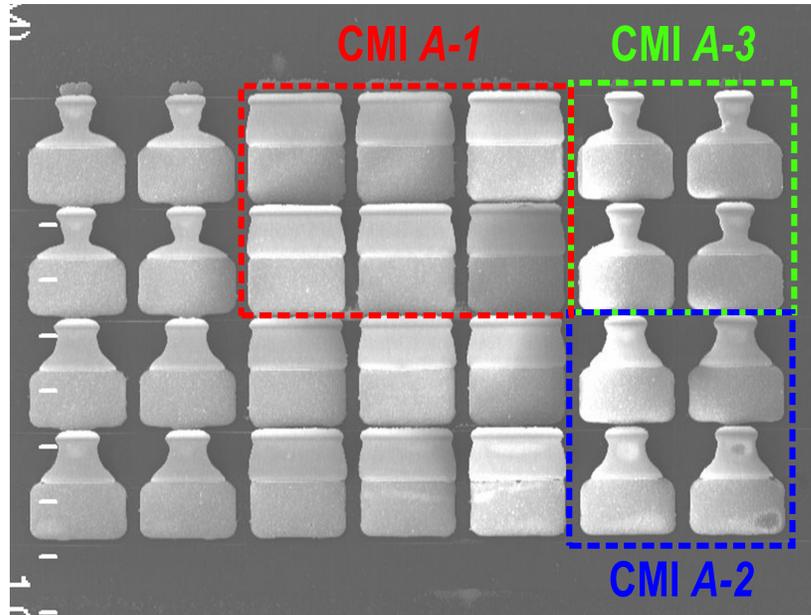


Figure 71 SEM images of the fabricated multi-height CMIs (CMI A)

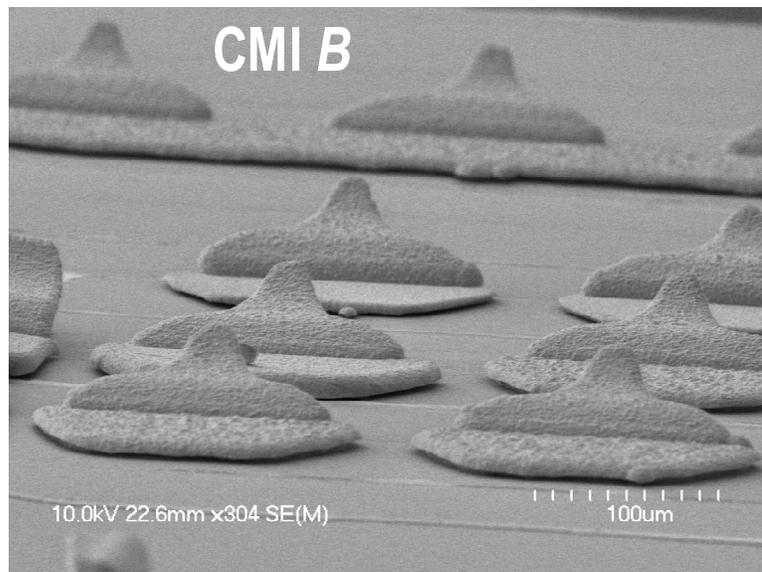
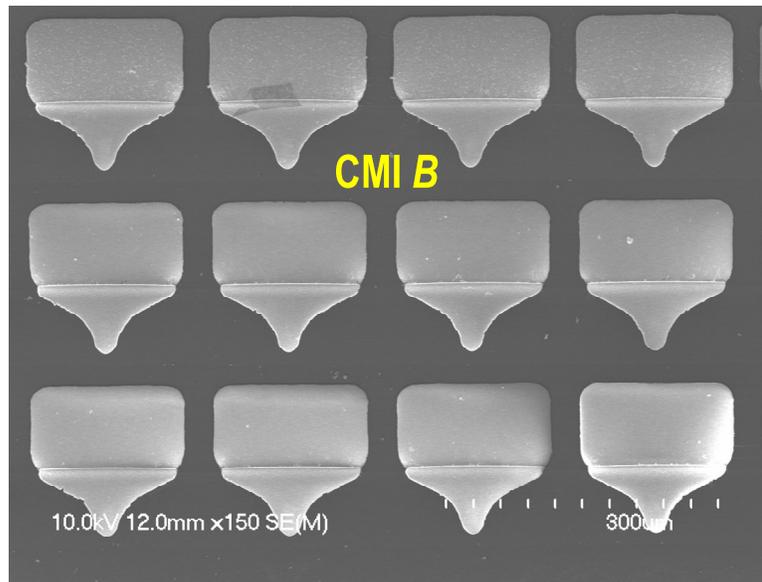
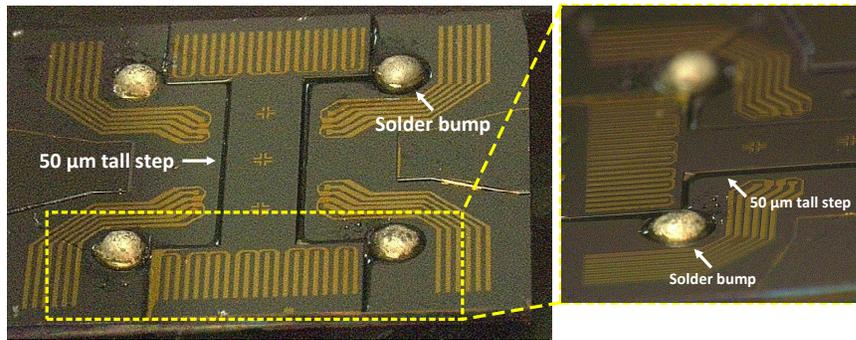
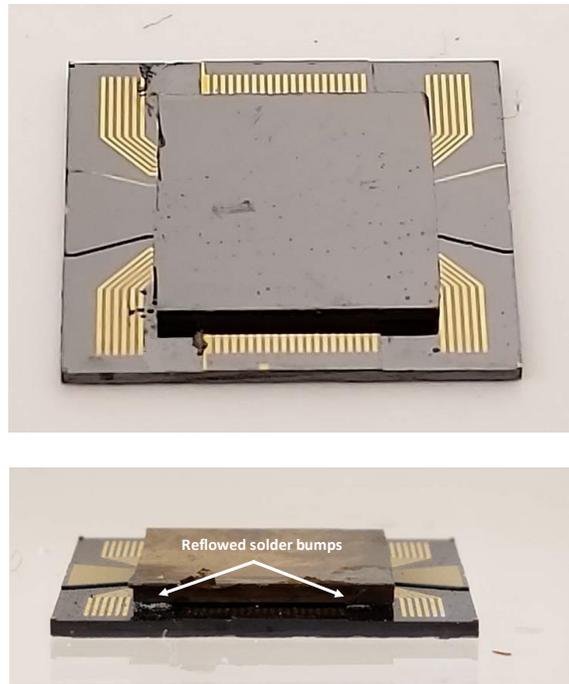


Figure 72 SEM images of the fabricated multi-height CMIs (CMI B)



(a)



(b)

Figure 73 Optical images of the testbed: (a) the silicon substrate with the step and solder bumps and (b) the assembled testbed

Figure 73 shows optical images of the fabricated silicon substrate with emulated surface-embedded chips (and solder bumps) and the assembled testbed. In this testbed, the

Table 13 Assembly parameters

Assembly method	Thermocompression bonding																
Assembly force	2 N																
Assembly gap	60 μm																
Reflowing process profile																	
<table border="1"> <caption>Data points for the reflowing process profile</caption> <thead> <tr> <th>Time (s)</th> <th>Temperature (°C)</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td></tr> <tr><td>40</td><td>130</td></tr> <tr><td>100</td><td>180</td></tr> <tr><td>130</td><td>180</td></tr> <tr><td>170</td><td>250</td></tr> <tr><td>190</td><td>250</td></tr> <tr><td>210</td><td>0</td></tr> </tbody> </table>		Time (s)	Temperature (°C)	0	0	40	130	100	180	130	180	170	250	190	250	210	0
Time (s)	Temperature (°C)																
0	0																
40	130																
100	180																
130	180																
170	250																
190	250																
210	0																

step height is approximately 52 μm . Spherical solder balls with a diameter of 500 μm are manually attached and reflowed on the metal pads before assembly (though electroplating can be used to fabricate the solder bumps as well). Thermocompression bonding is used to assemble the dice. Once the anchor chip is aligned to the substrate, the solder balls are reflowed again to provide mechanical interconnection between the anchor chip and the substrate while maintaining approximately 60 μm of gap. A force of 2 N was applied during bonding with a maximum temperature of 250 °C. The 2 N force was enough to compress all the fabricated CMIs on the anchor chip while maintaining the 60 μm of gap; the force was calculated based on the total number of CMIs on the anchor chip and their compliance values. Table 13 summarizes the assembly parameters. Mechanical compliance of CMIs

was measured using a Hysitron Triboindenter. The measured results are shown in Figure 74, and average compliance was 2.42 mm/N, 3.86 mm/N, 6.1 mm/N, and 2.9 mm/N, respectively for CMI A-1, CMI A-2, CMI A-3, and CMI B designs. These results illustrate the simplicity of CMI mechanical compliance engineering through only photomask geometry re-design (though there are additional parameters that impact compliance including thickness, material, and three-dimensional curved geometry). The four-point resistances of the interconnections after assembly were measured using a Karl-Suss probe station. As shown in Figure 75, the four-point resistance values of CMI A-1 and CMI B were measured, and their average four-point resistance, including contact resistance with the gold pads, is 222.4 m Ω and 71 m Ω , respectively. We believe the contact resistance between the CMIs and the pads contributes to this difference in the average resistances; as shown in Figure 70, the 60 μm gap (between the silicon substrate and the anchor chip)

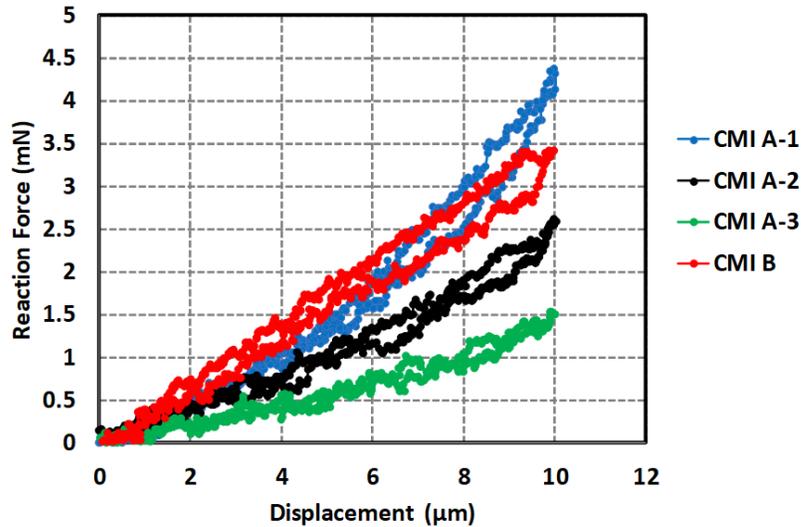


Figure 74 Force versus indentation displacement graph

Table 14 Dimension and mechanical and electrical characterization results of the fabricated multi-height CMIs

Interconnect	Pitch (μm)	Height (μm)	Compliance (mm/N)	Four-point resistance ($\text{m}\Omega$)
CMI A-1	200	65	2.42	222.4
CMI A-2			3.86	-
CMI A-3			6.1	-
CMI-B	200	35	2.9	71

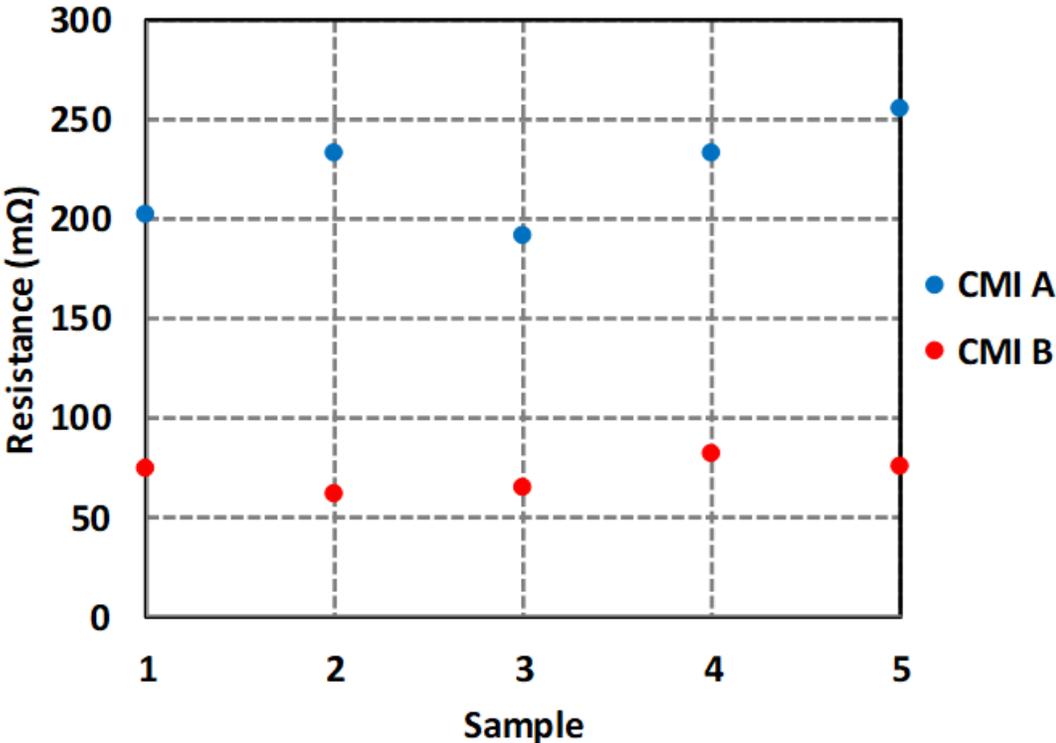


Figure 75 Four-point resistance of CMI A and CMI B

deforms the 65 μm tall CMI A by approximately 5 μm while the 8 μm gap (between the step and the anchor chip) deforms the 35 μm tall CMI B by approximately 27 μm ; this will affect the contact force and hence contact resistance of the CMIs. The deformation depth

and compliance of CMIs also determine the required thermocompression bonding force, which is discussed earlier in this section. For example, CMI A-1, CMI A-2, and CMI A-3 require 2.07 mN, 1.3 mN, and 0.82 mN, respectively, to deform down by 5 μm while CMI B requires 9.3 mN to deform down by 27 μm . Table 14 summarizes the compliance and four-point resistance characterization results and the dimensions of the fabricated multi-height CMIs.

6.2 Stitch-Chip Link RF Characterization

In order to gain initial insight into the frequency response of the CMIs in stitch-chip signal interconnection, a coplanar waveguide (CPW) with and without the CMIs were fabricated on a silicon substrate and measured. Figure 76 (a) shows the schematics of the CPW. A SiO_2 dielectric layer with 5 μm of thickness was used under the CPW. The Cu-Au TL is 9 μm wide and 2 μm in thickness. The 50 nm thick Au layer was deposited on top of the Cu layer to prevent oxidation. The spacing between the ground and signal line is 48 μm and the width of the ground line is 50 μm . The dimensions of the CPW are calculated to match to yield a characteristic impedance (Z_0) of 50 Ω . Pads with the dimension of 25 μm x 25 μm and the pitch of 50 μm are added to both ends of the transmission line for probing. The fabricated transmission lines were measured using an Agilent N5245A network analyzer from 10 MHz to 30 GHz. The measured S_{21} and S_{11} for transmission line (TL) lengths of 0.2 mm, 0.5 mm, and 1 mm are shown in Figure 76 (b). HFSS simulation results are compared with the measured results and show a good agreement. A clear trade-off between the loss and transmission line length can be observed. Next, CMIs with 50 μm pitch were fabricated on each end of the 1 mm long transmission lines, and RF characteristics of the stitch-chip channels through CMIs-TL-CMIs were measured by

directly probing the flat tip of the CMIs, as shown in Figure 77 (a). Figure 77 (b) shows the measured S_{21} and S_{11} results, and the insertion loss was 0.72 dB at 30 GHz while the reflection loss was lower than 10 dB through the whole 30 GHz range.

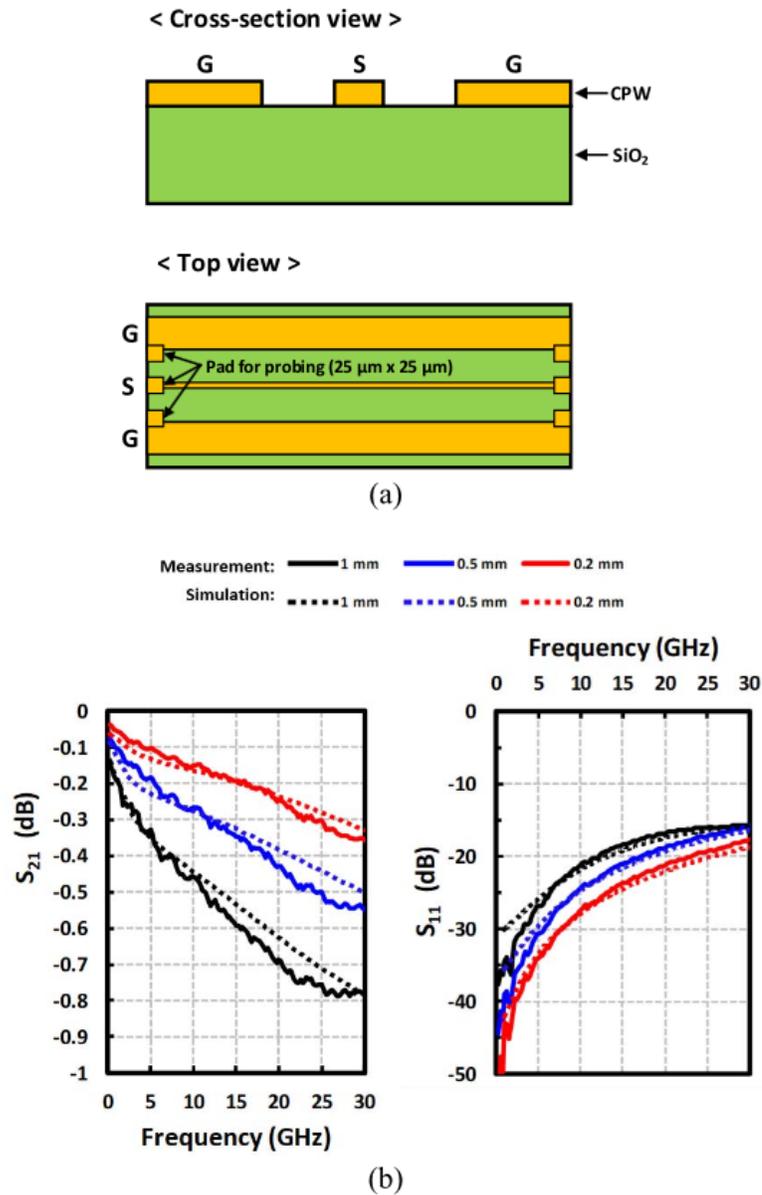
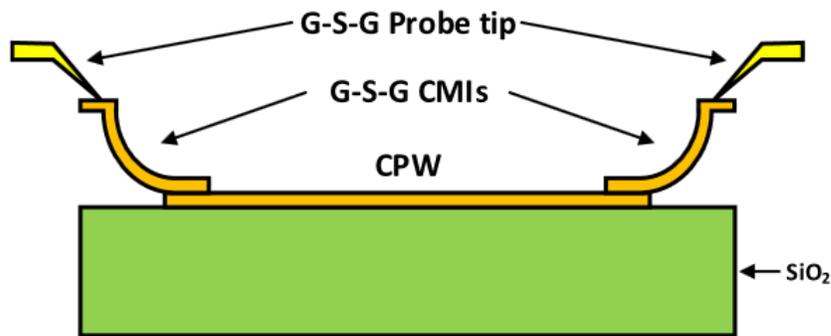
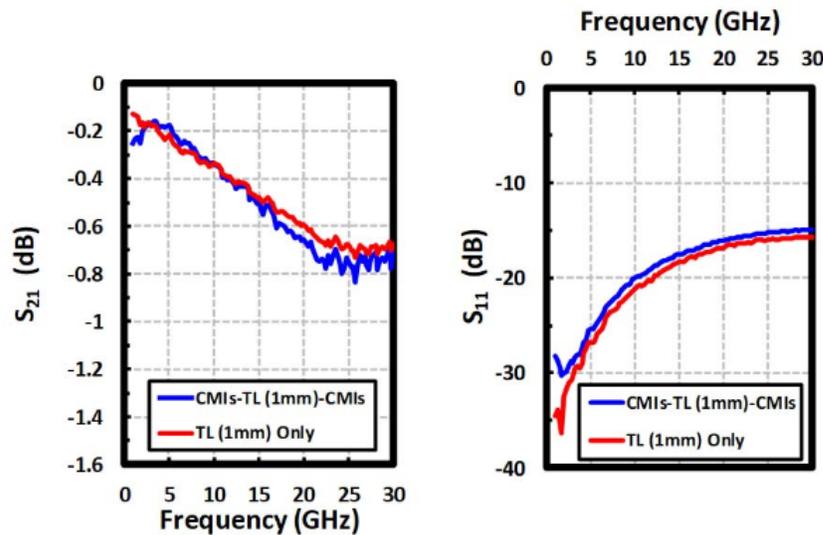


Figure 76 schematics of the CPW (a) and measured S_{21} and S_{11} of the CPW for three wire lengths



(a)



(b)

Figure 77 Schematic of the cross-section view of the measured CMI-TL (1mm)-CMI structure (a) and measured S_{21} and S_{11} results

As you can see from Figure 77, CMIs add very minor loss compared to the loss from TL, so if the length of TL is shorter than 1 mm (i.e., 0.2 mm or 0.5 mm TL, as shown in Figure 76), the insertion loss of interconnections through the stitch chip can be comparable to the insertion loss of TSVs from literatures [69-71]. Therefore, the proposed integration approach can provide low loss signal interconnections at high frequency.

6.3 Stitch-Chip Link Simulation

In order to characterize the high-frequency properties of the multi-height CMIs and the stitch-chip links both in aggregate form and individually, a carefully constructed testbed must be designed, fabricated, and experimentally tested to validate the models. In this section, we present the initial design and simulation results of such a testbed. Since the L-2L de-embedding method has been widely utilized for the characterization of transmission lines with TSV in the RF range [72], [73], our stitch-chip based high-frequency testbed is designed to be compatible with L-2L de-embedding.

Figure 78 shows the details of our ANSYS HFSS testbed model. The model contains a 2.5-D signal link, whose ABCD-matrix is denoted as [2.5D-Link] in Figure 78 (a). As shown in Figure 78 (a), this 2.5-D channel can be partitioned into a single CPW intermediate channel, two G-S-G pairs of CMIs whose ABCD-matrices are denoted as

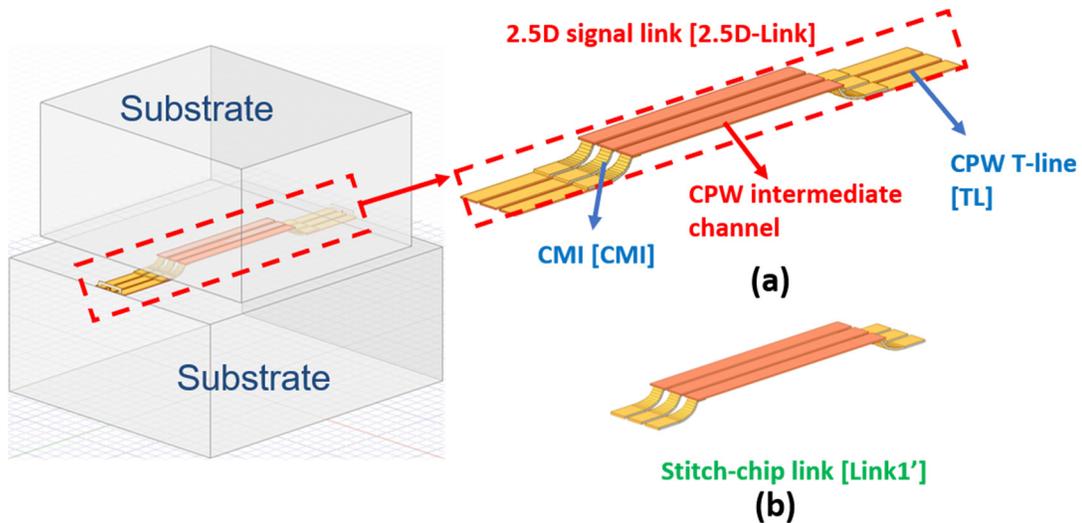


Figure 78 HFSS model of stitch-chip channel

[CMI] and two extended CPW T-line whose ABCD-matrices are denoted as [TL]. The two extended CPW T-lines can be de-embedded and the remaining structure, as shown in Figure 78 (b), is called the stitch-chip link whose ABCD-matrix is [Link1']. In practice, the tip of the CMIs would touch the CPW T-lines and deform elastically. However, this deformation is not accounted for in this work. L-2L de-embedding requires two 2.5-D signal links, one of which has an intermediate channel length twice as long as the other (ABCD-matrices [2.5D-Link1] and [2.5D-Link2]). [2.5D-Link1] and [2.5D-Link2] can be derived from the S-matrices measured from a vector network analyzer. After de-embedding the two extended CPW T-lines, the stitch-chip link's ABCD-matrix can be obtained. The procedure of this L-2L de-embedding can be summarized as follows [72], [73]:

$$[\text{Link1}'] = [\text{TL}]^{-1} [2.5\text{D-Link1}] [\text{TL}]^{-1} \quad (5)$$

$$[\text{Link2}'] = [\text{TL}]^{-1} [2.5\text{D-Link2}] [\text{TL}]^{-1} \quad (6)$$

$$[\text{CMI}] = \left(\sqrt{[\text{Link1}']^{-1} [\text{Link2}'] [\text{Link1}']^{-1}} \right)^{-1} \quad (7)$$

where [Link1'] and [Link2'] represent [2.5D-Link1] and [2.5D-Link2] after de-embedding the CPW T-lines at both ends. It should be noted that [Link1'] represents an ABCD-matrix of a stitch-chip link that consists of a CPW with CMIs on both ends. Thus, based on L-2L de-embedding, our designed testbed can potentially extract the electrical properties of both CMIs and stitch-chip links with high accuracy.

Table 15 Design points for different CMI versions

CMI design	AR = L/H	H (μm)	L (μm)	AL (μm)
60 μm tall CMI	2	60	120	145.3267
90 μm tall CMI	2	90	180	217.9901
90 μm tall CMI	1	90	90	141.3717

In the simulated testbed, the substrate material used for the stitch-chip is fused silica, which provides relatively low dielectric constant (~ 3.9) and loss tangent (~ 0.0002) within the RF range. The low dielectric constant and loss tangent enable low-loss transmission line design. Second, all CPWs are made using copper and their characteristic impedances are optimized to 50Ω . In Figure 78, the CPW intermediate channel will have two lengths, one of which is twice the other. The extended CPW T-line is fixed at $250 \mu\text{m}$ length while the total stitch-chip link has $500 \mu\text{m}$ -long CPW, as shown in Figure 78 (b). Lastly, several design versions for the CMIs have been included. Figure 79 illustrates the cross-sectional view of one nickel-core CMI (thickness varies from $5 \mu\text{m}$ to $7 \mu\text{m}$) coated with 500 nm -thick gold to avoid oxidation and to decrease resistance (DC and AC). Table

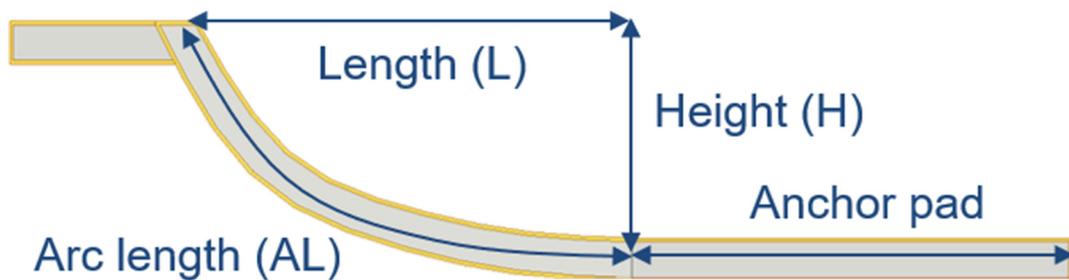


Figure 79 Cross-section view of CMI with design parameters

15 summarizes the key dimensions for different CMI designs. In Table 15, AR refers to the aspect ratio of the CMI and is defined as the ratio of the CMI's horizontal length (L)

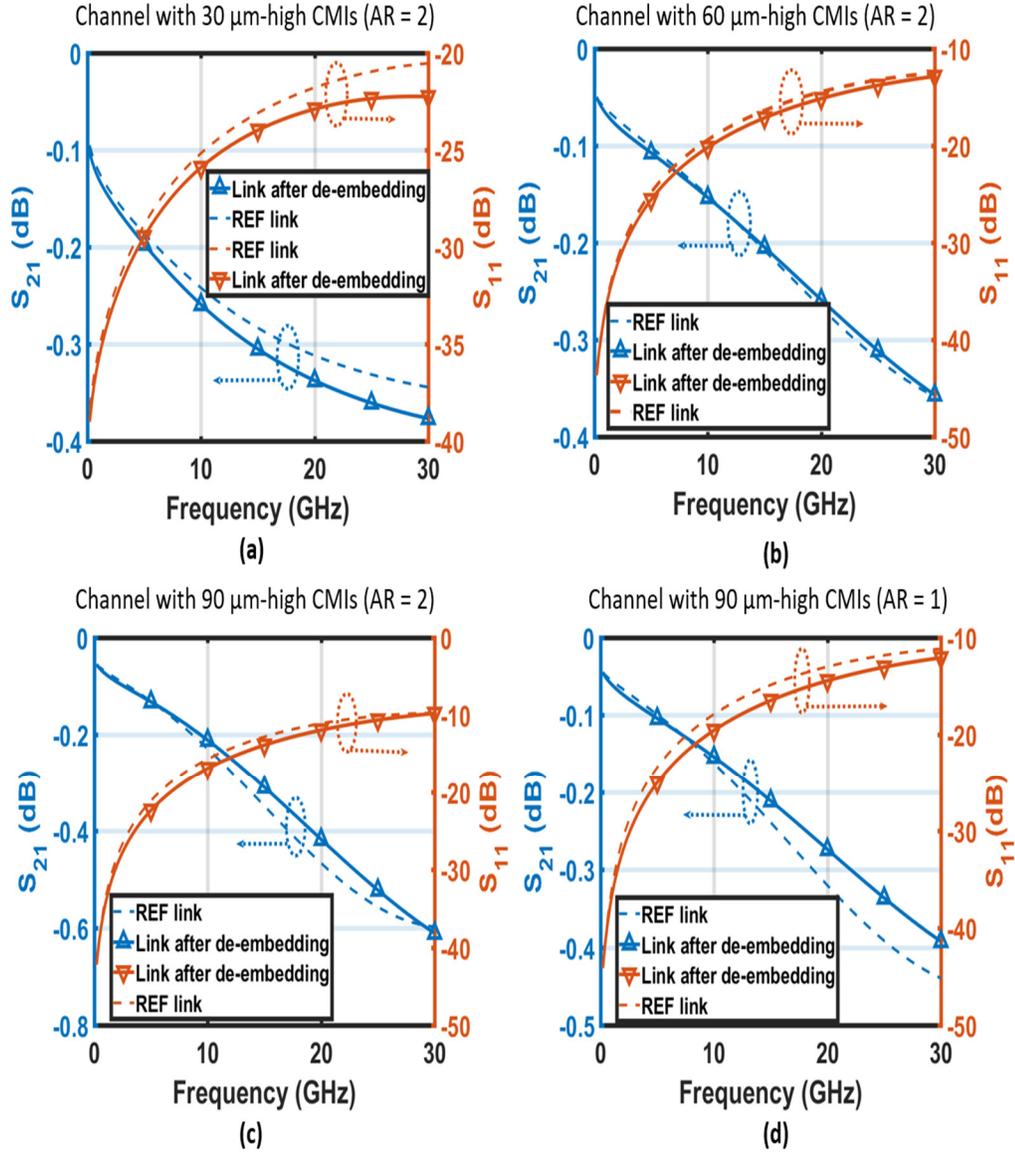


Figure 80 S-parameters results compared with standalone link (CMI+Tline+CMI). De-embedded link with (a) 30 μm -high CMIs (AR = 2); (b) 60 μm -high CMIs (AR = 2); (c) 90 μm -high CMIs (AR = 2); (d) 90 μm -high CMIs (AR = 1)

and vertical height (H) (see Figure 79). Arc length (AL) represents aggregate physical length of the CMI.

Simulations from DC to 30 GHz are conducted utilizing above models. Following conversion of S-matrices to ABCD-matrices and using model (5), an ABCD-matrix and S-matrix of the stitch-chip link (CMI+CPW+CMI) can be extracted. In order to validate the de-embedding method, a standalone case where a stitch-chip link has the same dimensions as the de-embedded stitch-chip link is set up as a reference (REF link). S_{21} and S_{11} for different stitch-chip link designs are shown in Figure 80. The magnitudes of the insertion loss (S_{21}) and the return loss (S_{11}) of the reference link and the testbed link after de-embedding are compared and show agreement. The stitch-chip links exhibit an insertion

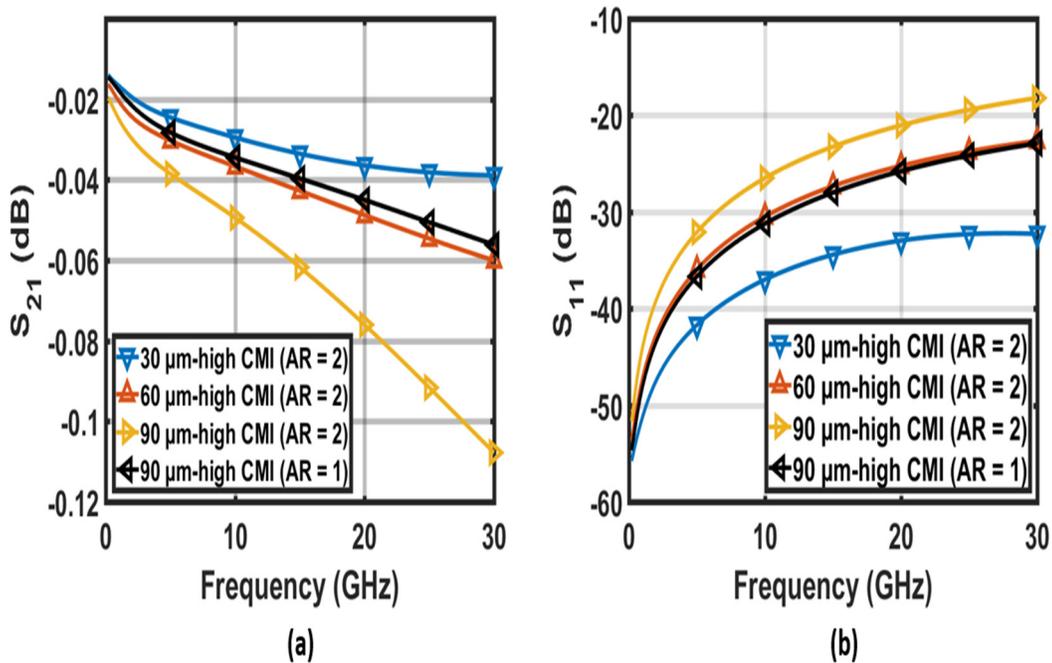


Figure 81 S-parameters comparison for CMIs with different heights: (a) Insertion loss and (b) Return loss

Table 16 Parasitics extraction @ 30 GHz for different CMIs

CMI design	R (mΩ/μm)	L (pH/μm)	G (μS/μm)	C (fF/μm)
60 μm tall CMI (AR = 2)	2.75	0.42	0.07	0.06
90 μm tall CMI (AR = 2)	2.2	0.45	0.03	0.06
90 μm tall CMI (AR = 1)	2.69	0.43	0.04	0.07

loss of less than 0.6 dB within 30 GHz and maintains good impedance matching (return loss better than -10 dB) even with largest CMIs (90 μm-high). Another objective of this testbed is to extract the electrical parasitics of the CMIs. After converting S-matrices to ABCD-matrices and following the models in (5) to (7), an ABCD-matrix and S-matrix of CMIs can be easily extracted [61]. Figure 81 shows the S_{21} and S_{11} for different CMI designs. As for S_{21} , CMIs provide low-loss 3-D interconnect solution within the RF range (insertion loss better than 0.11 dB). For S_{11} , CMIs still maintain acceptable impedance matching thanks to their electrically short structure. Note that by only reducing AR, the 90 μm-high CMI's loss is improved. The reason is that shrinking AR down from 2 to 1 results in approximately 35% reduction in physical length. Because of their short length relative to wavelength, a lumped model [34, 61, 74] can be used to extract RLGC parasitics. Table 16 summarizes the RLGC parasitics for some of the CMI designs at 30 GHz. Most of the CMI interconnect is surrounded by air, which results in low parasitic capacitance and conductance.

6.4 Conclusion

This chapter explores the fabrication and assembly process of a stitch-chip based polyolithic integration (HIST 3.0) enabled by multi-height CMIs. Experimental characterization of the proposed approach was performed by assembling the testbed using multi-height CMIs and surface-embedded chips emulated using a silicon step. The experimental results show that the multi-height CMIs can enable robust electrical interconnection irrespective of off-chip interconnection distance differences. These results demonstrate a new degree of freedom in system-level integration when compared to conventional solder bumps. In this chapter, we also present HFSS-based simulations of the CMIs and stitch-chips to gain initial insight into their high-frequency response.

CHAPTER 7. SUMMARY AND FUTURE WORK

7.1 Summary of the Thesis

The objective of this research is to experimentally demonstrate dense compliant interconnects, which we call Compressible MicroInterconnects (CMIs), and explore a polyolithic integration of heterogeneous dice using the CMIs.

7.1.1 *Compressible MicroInterconnects (CMIs)*

We developed a highly flexible and elastically deformable first-level interconnect, which we call Compressible MicroInterconnects (CMIs). The key features of the CMI technology include: 1) lithographically-defined, CMOS-compatible and simple fabrication, 2) large elastic range of motion to compensate for surface non-uniformity on the attaching substrate, especially for large die or interposer assembly, and CTE mismatch induced warpage, 3) high-degree of freedom in interconnect design, 4) pressure-based and non-permanent contact mechanism to provide temporary interconnections, 5) CMIs eliminate the rolling effect when they deformed, and thus maintain electrical contact points, and 5) since thermo-compression process is not required, the assembly process is simplified as bonding parameters such as temperature may not be considered.

The CMIs, with an in-line pitch of 150 μm and height of 80 μm , were fabricated and demonstrated up to 45 μm vertical range of motion within the elastic region. In addition, CMIs with two different thicknesses (7.6 μm and 10.5 μm) were fabricated for electrical & mechanical characterization. The measured compliance of the 7.6 μm and 10.5 μm thick CMIs is 13.12 mm/N and 9.34 mm/N, respectively. The average four-point resistance,

including contact resistance with a gold pad, of the 7.6 μm thick CMIs is 226.1 $\text{m}\Omega$ and that of the 10.5 μm thick CMIs is 176.3 $\text{m}\Omega$.

In order to meet the increasing need for higher I/O densities for increasing signal bandwidth requirements, fine-pitch CMIs were demonstrated. In addition, in order to address potential non-uniform bonding force issue that could be introduced by assembly with a substrate with relatively large surface non-uniformity (potentially because of chip thickness differences or a die pre-attached on the substrate), multi-height CMIs were proposed and demonstrated. The fabricated multi-height CMIs are approximately 75 μm , 55 μm , and 30 μm tall, and their in-line pitch is 150 μm . One of the 75 μm tall CMIs was consecutively indented for 5,000 cycles to test their lifetime fatigue reliability. Their measured respective compliances were 12.21 mm/N , 8.82 mm/N , and 3.91 mm/N . Four-point resistance was measured by directly probing the multi-height CMIs. The average resistance of the 75 μm , 55 μm , and 30 μm tall CMIs was 67.17 $\text{m}\Omega$, 55.18 $\text{m}\Omega$, and 48.13 $\text{m}\Omega$, respectively. The fabricated fine-pitch CMIs have 30 μm x 30 μm pitch and are approximately 9.5 μm tall and 2.5 μm thick. Down to 1 μm thick fine-pitch CMIs have been fabricated as well. The fabrication of the very thin CMI confirms the capability of a wide range of compliance design. The multi-height and fine-pitch CMIs are important especially for a polyolithic multi-die integration technology, which we call Heterogeneous Interconnect Stitching Technology (HIST).

7.1.2 Polyolithic Integration of 2.5-D and 3-D Chiplets Enabled by Heterogeneous Interconnect Stitching Technology (HIST) with CMIs

We propose HIST 1.0 platform to enable the interconnection of multiple dice (or “chipllets”) of various functionalities in a manner that mimics monolithic-like performance, yet utilizes advanced off-chip interconnects and packaging to provide flexibility in IC fabrication and design, improved scalability, reduced development time, and reduced cost. In HIST 1.0 platform, a stitch-chip with high-density fine pitch wires is placed between the substrate and the chipllets. Fine-pitch microbumps are used to bond chipllets to the stitch-chip to provide high-bandwidth density and low-energy signaling. CMIs are used to compensate for package non-planarity and enable chipllet-package interconnection. Compared to competitive solutions, HIST achieves a similar signal bandwidth density as the silicon interposer technology, but is not reticle-size limited, thus making it very scalable in size. In addition to this, HIST eliminates the need for TSVs in the substrate for decreased cost and improved signaling. HIST is also based on die-to-die face-to-face bonding, and thus there are no intermediate package levels as in the case for EMIB, which enables higher signal I/O pitch and lower capacitance. Lastly, HIST can be applied to any packaging substrate (organic, ceramic, etc.) since HIST is augmented to the top-most surface of the package substrate. The testbed for HIST 1.0 was fabricated, assembled, and characterized for the first time. The testbed features of fine-pitch (down to $10\ \mu\text{m} \times 10\ \mu\text{m}$) and $5\ \mu\text{m}$ tall Au-Cu microbumps and CMIs with $200\ \mu\text{m}$ in-line pitch and $55\ \mu\text{m}$ height. Mechanical compliance of the CMIs is approximately $13.7\ \text{mm/N}$, and CMIs can achieve up to $30\ \mu\text{m}$ of vertical elastic deformation. The post-assembly resistance values of the $20\ \mu\text{m} \times 20\ \mu\text{m}$ pitch microbumps ranges from $77.8\ \mu\Omega$ to $188.3\ \mu\Omega$, and the resistance of the CMIs (including contact resistance) ranges from $141.2\ \text{m}\Omega$ to $252.9\ \text{m}\Omega$.

After the demonstration of HIST 1.0, we further advanced the HIST 1.0 approach and developed HIST 2.0 with fine-pitch CMIs. We replaced the fine-pitch microbumps of HIST 1.0 with CMIs featuring 20 μm in-line pitch to enable large-scale heterogeneous integration. Solder bumps with 50 μm height and 200 μm x 200 μm pitch are used for power delivery, signal routing between a die and package, and mechanical interconnection between anchor chips and a package substrate. The testbed for HIST 2.0 was fabricated, assembled, and characterized. Chips containing fine-pitch CMIs were flip-chip bonded onto three substrates containing different stitch-chip thickness mismatches ($\Delta t = 0 \mu\text{m}$, 10 μm , and 20 μm) to demonstrate the flexibility of CMIs on stitch-chip thickness variation or surface non-planarity of a substrate. The average resistance of the CMIs after assembly is 146.31 m Ω , 170.02 m Ω , and 176.71 m Ω , respectively for $\Delta t = 0 \mu\text{m}$, 10 μm , and 20 μm thickness mismatch. The average resistance of the solder bumps is 1.31 m Ω . These four-point resistance measurement results confirm that the CMIs can maintain electrical connections between the die and the stitch-chips even when there is a stitch-chip thickness mismatch resulting perhaps from using dice from different foundries.

An advanced polyolithic integration technology (HIST 3.0) enabled by multi-height CMIs is proposed and demonstrated. We replaced all off-chip interconnects with fine-pitch and multi-height CMIs to potentially provide replaceability of assembled dice. Since the CMIs are elastically compressible unlike conventional solder bumps, the proposed polyolithic integration technology can compensate for any possible off-chip interconnection distance differences resulting from chip thickness differences; this can enable both 2.5-D and 3-D face-to-face interconnection in one platform. In the HIST 3.0 testbed, the surface-embedded chip on the package substrate is emulated by forming a tall step on the silicon

substrate. Four solder bumps are also fabricated on the silicon substrate to mechanically secure the assembled testbed. For the anchor chip with multi-height CMIs, two CMI designs with different heights, which we refer to as CMI A and CMI B in this thesis, are fabricated on a silicon substrate. Both CMI A and B designs are formed on a $200\ \mu\text{m} \times 200\ \mu\text{m}$ pitch while the heights are approximately $65\ \mu\text{m}$ and $35\ \mu\text{m}$, respectively. The four-point resistance values of CMI A and CMI B were measured, and their average four-point resistance, including contact resistance with the gold pads, is $222.4\ \text{m}\Omega$ and $71\ \text{m}\Omega$, respectively. HFSS RF simulation of stitch-chip links exhibit an insertion loss of less than $0.6\ \text{dB}$ within $30\ \text{GHz}$ and maintains good impedance matching (return loss better than $-10\ \text{dB}$) even with largest CMIs ($90\ \mu\text{m}$ -high).

7.2 Future Work

The potential opportunities to advance this dissertation work will be discussed in this section.

7.2.1 RF characterization of HIST channels and CMIs

The potential applications of HIST platform include integration of RF components into a single package. For RF/analog applications, the high frequency performance of HIST channels are of particular interest. Even though HFSS RF simulations were conducted for CMIs and HIST channels, it is critical to experimentally verify the simulation results. Therefore, a testbed for RF characterization of the HIST channels through stitch-chips could be fabricated and measured. Since the stitch-chip can be formed using a variety of substrate materials depending on application, stitch-chip with quartz substrate could be used as an example due to its low-substrate loss, which is key in high-speed digital and

mm-wave transmission. In addition to this, advanced testbeds may be designed to characterize the high-frequency performance and RLGC of multi-height CMIs. Although we extracted the inductance and capacitance of the CMIs, there are other more parameters to explore that can impact the RF performance of CMIs, which include pitches, heights, materials, and deformation depths.

7.2.2 Thermomechanical reliability test of HIST platform

As mentioned earlier in this thesis, CMIs can improve thermomechanical reliability of the HIST platform as they can absorb strain from warpage that can be introduced by mismatch in coefficient of thermal expansion (CTE). Therefore, it is also important to demonstrate the improved thermomechanical reliability of the HIST platform. In order to verify the improved thermomechanical reliability, separate testbeds with different interconnects, such as CMIs and microbumps, can be fabricated and tested.

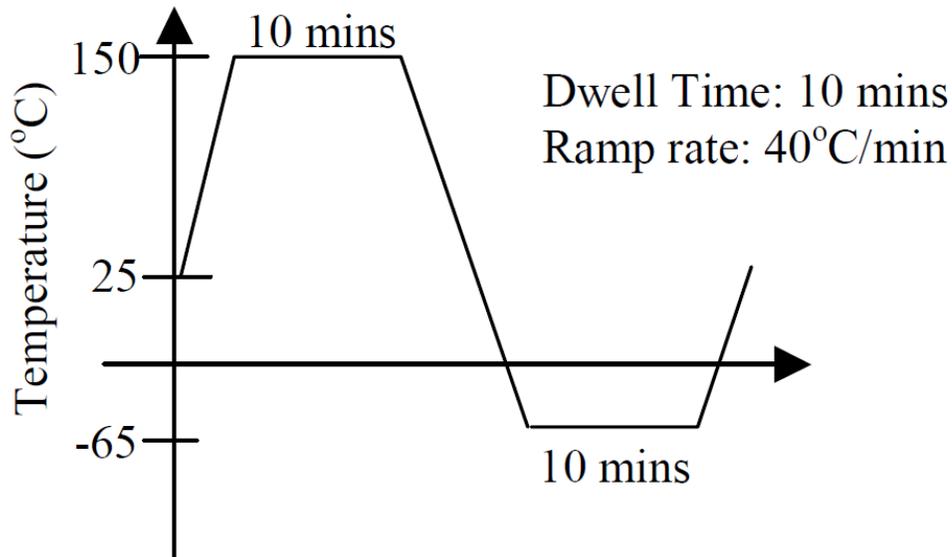


Figure 82 Temperature cycling profile

Thermomechanical reliability of a package system is often characterized through accelerated thermal cycling tests. The thermal cycling test can be subjected to the temperature cycling profile as per JEDEC Standard of -65 °C to +150 °C, with 2 cycles/hour, upper and lower soak times of 10 minutes, as shown in Figure 82 [78]. After the thermal cycling test, four-point resistance measurement can be carried out to verify any interconnection failures by CMIs or microbumps. In addition to this, visual inspection of cross-section of the testbeds can be conducted to examine any interconnect joint interface.

7.2.3 HIST platform demonstration with active dice

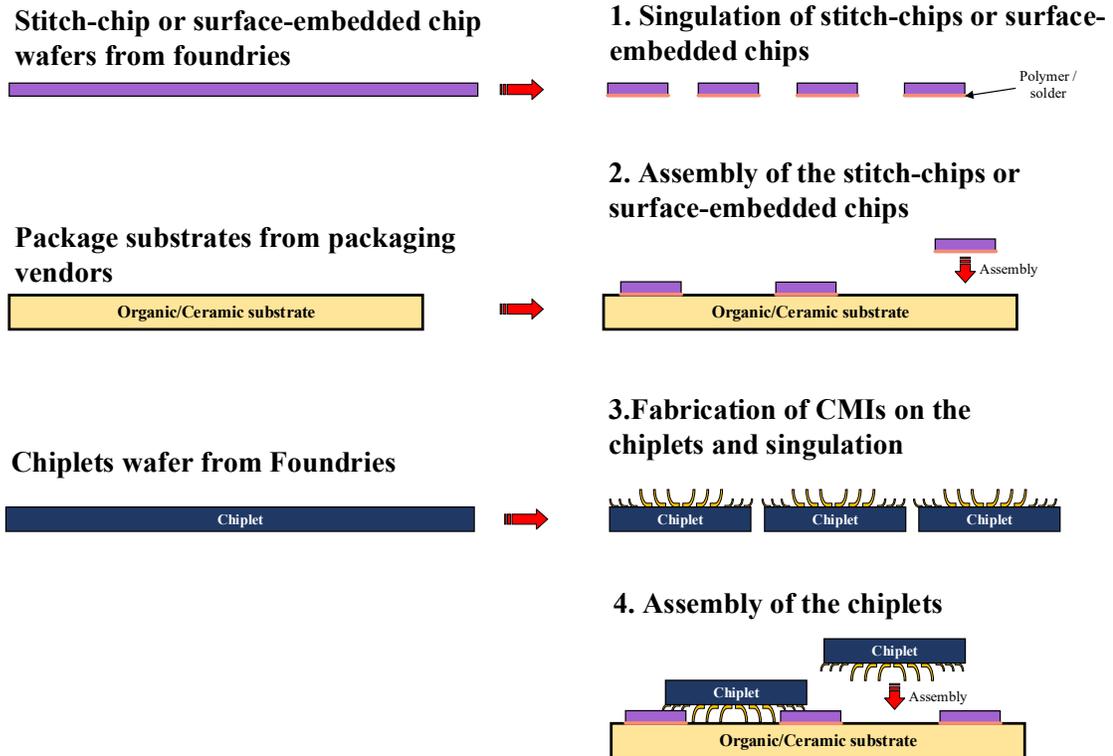


Figure 83 Demonstration of HIST platform with active dice

Although the HIST platform has been demonstrated and characterized through multiple testbeds, the potential of this technology has not been fully shown. Demonstrations with active circuitry can further demonstrate the capability of the HIST platform. A potential next step is the assembly of active dice using HIST on various package substrates (organic, ceramic, etc.), as shown in Figure 83. In this demonstration, stitch-chips or surface-embedded chips can be assembled on a package substrate using adhesive material (e.g. polymer or solder). Next, CMIs can be fabricated on chiplets at wafer form prior to singulation. Note, CMIs can also be fabricated on stitch-chips. Finally, active dice or chiplets can be assembled on the package substrate and tested. Large solder bumps for mechanical assembly can be placed either on the chiplet wafers or the package substrate before the final assembly.

7.2.4 HIST platform with photonic dice

Another vision of the HIST platform is to build a large scale system with subsystems that have high density electrical interconnections within a module and high-

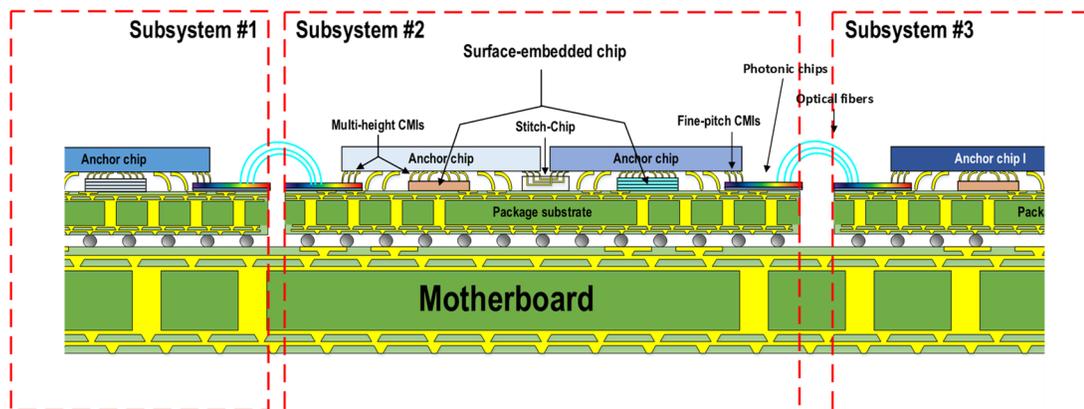


Figure 84 HIST platform with photonic dice

bandwidth optical links to communicate with other subsystems, as shown in Figure 84. In the HIST platform, the photonics receiver can be integrated into the stitch-chips or assembled in the system as an anchor chip. All data transferred to the photonics receiver can be transmitted through the high density fine-pitch CMIs to the subsystem. In this platform, the motherboard will only carry limited number of signals while most of the data traffic can be transmitted via the optical fibers.

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